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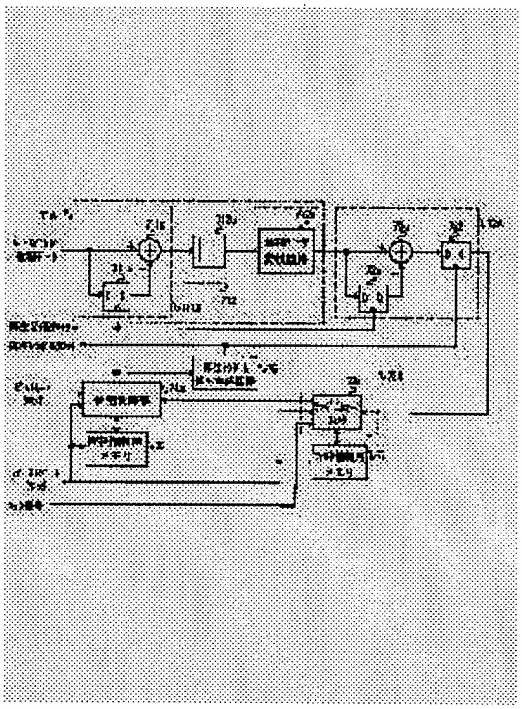
(54) TIMING REGENERATION CIRCUIT AND DEMODULATOR USING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To attain high-speed phase locking and low jitter of a timing phase after locking, while operating a timing regenerating means and a demodulator using it at a frequency twice the symbol rate or at a frequency equivalent to a symbol rate.
SOLUTION: This timing recovery means is made up of a symbol frequency component generating means 71A that generates a data series, including a symbol frequency component is a timing twice the symbol rate from base band phase data subject to oversampling at a rate twice the symbol rate and a phase control means 74A that realizes phase control of a regenerated clock at an interval of a phase control step, sufficiently smaller that the symbol period, while receiving a close signal with a fixed frequency twice the symbol rate.



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NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] About a timing regenerative circuit and a demodulator, especially this invention has a high bit rate, and can be applied to the demodulator of the digital high-speed radio device using an PSK (Phase Shift Keying) modulation technique.

[0002]
[Description of the Prior Art] Examination of pi / timing playback system for 4 shift QPSK using reference "input-signal topology as a timing regenerative circuit of the demodulator for digital radio devices using a former and PSK modulation technique" (there is what realizes high-speed phase level luffing motion with the feedback mold which samples phase data by 4 times of a symbol rate as indicated by the Institute of Electronics, Information and Communication Engineers synthesis convention B-450 in 1996 written by Toson.) A Prior art is explained using a Fig. below. The conventional demodulator which included the above-mentioned timing regenerative circuit in drawing 22 is shown. In drawing, 1 is [a rectangular detector circuit the fixed clock generator for timing playback a timing regenerative circuit and whose 8 a polar-coordinate conversion circuit and 6 are / 3 / the local oscillator for rectangular detection and 4 / for a sampling circuit and 5 / 16 times the frequencies of a symbol rate as for a data judging circuit and 7, four a1, and 4b of a limiter and 2] A-D converters.
[0003] Next, actuation is explained based on drawing. Here, let modulation techniques be pi / 4 shift differential coding QPSK modulation technique. A limiter 1 carries out amplitude limiting of the receiving IF signal. The rectangular detector circuit 2 carries out rectangular detection using the local signal which has the same frequency as the center frequency of the IF signal outputted from the local oscillator 3 for rectangular detection in the IF signal by which amplitude limiting was carried out, and is changed into a baseband inphase signal and a baseband rectangular cross signal. A-D converters 4a and 4b which constitute a sampling circuit 4 carry out the AD translation of a baseband inphase signal and the baseband rectangular cross signal using playback 4 clock-doubling 4 times the frequency of the symbol rate supplied from the timing regenerative circuit 7, and output the exaggerated 4 time sample data after an AD translation as baseband inphase data and baseband rectangular cross data. This baseband inphase data and rectangular data are inputted into the polar-coordinate conversion circuit 5. The polar-coordinate conversion circuit 5 carries out polar-coordinate conversion of the baseband inphase data from a sampling circuit 4, and the baseband rectangular cross data, and outputs them as an inphase and rectangular baseband phase data.
[0004] The timing regenerative circuit 7 performs phase control of playback 4 clock-doubling, and phase control of the playback symbol clock for extracting the phase data of a nyquist point in the data judging circuit 6 so that the nyquist point of a baseband inphase and a rectangular signal may be sampled from the baseband phase data of the output of the polar-coordinate conversion circuit 5. Moreover, the timing regenerative circuit 7 needs a fixed clock 16 times the frequency of a symbol rate in order to perform phase control of each clock at intervals of 1 / 16 symbol steps. This fixed clock is supplied from the fixed clock generator 8 for timing playback. The data judging circuit 6 extracts the phase data of a nyquist point from the baseband phase data from a sampling circuit 4 using the playback symbol clock reproduced in the timing regenerative circuit 7. And differentially coherent detection is performed using the phase data of the extracted nyquist point, and recovery data are outputted. Thus, since the demodulator indicated as this conventional example is the configuration of the feedback mold which operates using the receiving PSK signal by which amplitude limiting was carried out, and performs an AD translation to the timing of playback 4 clock-doubling, it can be constituted from an easy circuit which has a limiter in the preceding paragraph, and can realize the miniaturization of a circuit.
[0005] Drawing 23 is drawing showing the detailed configuration of the timing regenerative circuit in drawing 22 . 71 the complex multiplication section and 73 for the symbol frequency component generation section and 72 The low-pass filtering section, 74 consists of the phase control sections. A phase contrast part circuit and 712 further 711 A data-conversion circuit, 711a, 711b, 72a, 72b, 72e, and 72f A D flip-flop, 711c, 72c, and 72d -- for a phase data-conversion circuit, and 73a and 73b, an integrating filter and 73c are [a subtractor and 712a / an absolute value conversion circuit and 712b / an integrating filter control circuit and 74a of an arc tangent circuit and 73d] 4-bit down counters. Next, actuation of the timing regenerative circuit 7 is explained with reference to drawing. From baseband phase data theta (t) by which the PSK modulation was carried out, symbol frequency component deltatheta (t) which has DC offset is generable by the following formulas (1a). However, a symbol period is set to T.
deltatheta(t) =min {|theta(t)-theta(t-T/2) | and 2pi-|theta(t)-theta(t-T/2) |} (1a)
deltatheta (t) generated by drawing 24 as an example from baseband phase data [of the random pattern by which pi / 4 shift

QPSK modulation was carried out] theta (t), and theta (t) is shown. O The mark is nyquist point data. An axis of abscissa is time amount and a unit is the symbol period T. An axis of ordinate is a phase and a unit is a radian. Since it is pi / 4 shift QPSK modulation technique, the phase transition between the nyquist points of baseband phase data theta (t) is ** pi/4, and **3pi/4. It turns out that the symbol frequency (fs) component (sin2pifs (t) +A) of a transmitting side which the DC offset A shown by the dotted line produced is included in deltatheta (t) so that drawing 24 may also show.

[0006] In the conventional timing regenerative circuit 7, in order for the operation based on DFT (Discrete Fourier Transform) to perform timing phase presumption, it is necessary to carry out the sample of theta (t) at a rate 4 times the sampling rate of a symbol. Therefore, in the conventional timing regenerative circuit 7, theta (t) is obtained by the discrete data theta (iT/4) shown in a formula (1b) (however, i= {1, 2, 3, --}). The symbol frequency component generation section 71 generates data sequence deltatheta (iT/4) containing a symbol frequency component by the following formulas (1b) from the input baseband phase data theta (iT/4) by which the exaggerated sample was carried out by 4 times of a symbol rate.

deltatheta(iT/4) = min {|theta(iT/4)-theta(i-2) (T/4) | and 2pi-|theta(iT/4)-theta(i-2) (T/4) |} (1b)

The phase contrast part circuit 711 performs difference of theta(iT/4)-theta (i-2) (T/4) of a formula (1). This processing is realizable by carrying out difference of the phase data delayed by 2 sampling-time D flip-flops 711a and 711b using subtractor 711c from current phase data. Moreover, absolute value conversion circuit 712a carries out absolute value conversion of this phase contrast part value, phase-angle data-conversion circuit 712b is which of the value which subtracted the phase-angle data by which absolute value conversion was carried out, and the phase-angle data by which absolute value conversion was carried out from 2pi by the radian display, or it being small, while outputting, and processing of the above-mentioned formula (1) is realized. In addition, phase data-conversion circuit 712b can consist of a subtractor and a comparator easily.

[0007] The complex multiplication section 72 searches for correlation for one symbol with deltatheta (iT/4) containing the frequency component fs of this transmitting side, and the symbol frequency by the side of a receiver (fs**') with the following formulas (2a) and (2b). CI (the inphase component of a correlation value [in / in jT) / j (= 1, 2, 3, --) symbol eye] and CQ(jT) is the orthogonal component of the correlation value in j (= 1, 2, 3, --) symbol eye.

[0008]

[Equation 1]

$$CI(jT) = \sum_{i=4j-3}^{4j} \Delta\theta(iT/4) \times \cos 2\pi fs'(iT/4) \qquad (2a)$$

$$CQ(jT) = \sum_{i=4j-3}^{4j} \Delta\theta(iT/4) \times \sin 2\pi fs'(iT/4) \qquad (2b)$$

[0009] the above cos2pifs** (iT/4) -- 1, 0, -1, 0 and 1, and -- a repeat -- it is -- the above-mentioned sin2pifs** (iT/4) -- 0, 1, 0, and - 1, 0, and -- since it is a repeat -- Above CI (jT) -- CQ, (jT) can be easily calculated by the following formulas (3a) and (3b).

CI(jT) =deltatheta(3jT/4)-deltatheta (4j-2) (T/4) (3a)

CQ, (jT) =deltatheta(4j-3) (T/4)-deltatheta (4j-1) (T/4) (3b)

In an actual circuit, CI (jT) subtracts current deltatheta (iT/4) by subtractor 72c, is latching the data after subtraction by D-flip-flop 72e which operates in the start of a playback symbol clock, and is easily obtained from deltatheta (iT/4) latched by D-flip-flop 72a which operates in the start of playback 2 clock-doubling. It is obtained easily [similarly] by CQ(jT) subtracting deltatheta (iT/4) latched by 72f of D flip-flops which operate in the fall of playback 2 clock-doubling from deltatheta (iT/4) latched by D-flip-flop 72b which operates in the fall of playback 2 clock-doubling by 72d of subtractors, and latching the data after subtraction by D-flip-flop 72e which operates in the start of a playback symbol clock.

[0010] Next, first, integrating filters 73a and 73b are used for the low-pass filtering section 73, it equalizes CI(jT) CQ(jT), removes a noise component etc., and outputs the signal after equalization as DI (jT) and DQ (jT). An integrating filter uses the following formulas (4a) and the filter of the infinity impulse response mold which operates by (4b). However, alpha is an oblivion multiplier and takes the range of (0< alpha<1).

DI(jT) = DI(j-1) (T) xalpha+CI (jT) (4a)

CQ [+ / DQ(jT) = DQ(j-1) (T) xalpha] (jT) (4b)

[0011] Next, in arc tangent circuit 73c, the vector angle deltathetaj which DI (jT) and DQ (jT) show is searched for by the following formulas (5).

deltathetaj =tan-1 (DQ(jT) / DI (jT)) (5)

This vector angle deltathetaj Since it is the phase contrast of symbol frequency component sin2pifs (t) and symbol frequency component fs** of a receiving side which are contained in the phase data of a transmitting side, the following formulas (6) are realized.

sin2pifs(t) =cos (2pifs** (t)+deltathetaj) (6)

therefore, this deltathetaj from -- the phase correction value Ej which negates a timing phase error can be calculated.

[0012] At 73d of integrating filter control circuits, only when becoming the multiple of the time amount k with the symbol time amount j, the phase error Ej and a control instruction signal are outputted. That is, the phase correction value Ej and a control instruction signal are outputted at intervals of k symbol. The phase control section 74 is made to run by himself with the 16 time symbol rate clock which is a clock of operation, unless it consists of for example, 4-bit down counter 74a and the phase correction

value Ej and a control instruction signal are inputted. From the most significant bit of this 4-bit down counter 74a to the 3rd bit is outputted as a playback symbol clock, playback 2 clock-doubling, and playback 4 clock-doubling, respectively. Moreover, if the phase correction value Ej and a control instruction signal are inputted into the phase control section 74, the synchronous load of the phase correction value Ej will be carried out at 4-bit down counter 74a. In this example, timing of a synchronous load is taken as the timing which shows "0" at the time of 4-bit down counter 74a running by itself.

[0013] An example of this actuation is shown in drawing 25 . In time amount A, the timing phase error of the playback symbol clock start and a nyquist point is produced -3pi/8. - In order to negate the timing phase error of 3pi/8, the low-pass filtering section 73 will give the instruction advanced 3T / 16 (T: symbol period) by each processing mentioned above, if the phase of a playback clock is made into 3pi/8 and time amount. In this case, in the time amount B which shows "0" at the time of 4-bit down counter 74a running by itself, the low-pass filtering section 73 outputs phase correction value Ej=3 and a control instruction pulse (logic "1"), respectively (if the phase correction value Ej is loaded, the clock phase amended will be set to Ejpi/8). 4-bit down counter 74a carries out the synchronous load of the phase correction value Ej, when a control instruction signal shows logic "1." In time amount C, the start point and nyquist point of a playback symbol clock are in agreement, and the data of a nyquist point are sampled by the above-mentioned processing after time amount C. Moreover, if a control instruction signal shows logic "1", an integrating filter will perform control of the following formulas (7) to an integrating filter.

[0014]

[Equation 2]

$$DI(jT) \leftarrow \sqrt{DI((j-1)T)^2 + DQ((j-1)T)^2}$$

$$DQ(jT) \leftarrow 0 \qquad (7)$$

[0015] Since after the 1st phase control can use an integrating filter, the feedback mold timing regenerative circuit which performs high-speed level luffing motion using an integrating filter is realizable with this control. this ** -- like, since the conventional timing regenerative circuit 7 searches for a timing phase error from the vector angle which the correlation value of deltatheta (t) containing the frequency component fs of a transmitting side and the symbol frequency by the side of a receiver (fs**) shows, it can realize a high-speed phase level-luffing-motion property.

[0016]

[Problem(s) to be Solved by the Invention] As mentioned above, this multiplication is not materialized unless it asks for deltatheta (t) to the timing of being 4 times much as a symbol rate, at least, since the conventional timing regenerative circuit 7 needs to carry out the multiplication of the cosine component and sign component of a symbol frequency by the side of a receiver to deltatheta (t), respectively. Therefore, in the timing regenerative circuit 7, there is the need of carrying out over sampling technique of the baseband data by 4 times of a symbol rate.

[0017] Moreover, by the control section 74, since at least conventional one has the need of making sufficiently small the phase control number of steps of a playback clock, the need that the conventional phase control section 74 operates with a clock 16 times the frequency of a symbol rate has it.

[0018] On the other hand, the communication system which realizes the radio transmission by the high symbol rate of dozens of or more Mbauds in recent years is in the limelight. If it uses for such a high-speed radio communications system, since the over sampling technique frequency of data and the clock frequency of the phase control section 74 will become very high with dozens of MHz - hundreds of MHz, the increment in the power consumption of a receiver produces the conventional timing regenerative circuit 7. Moreover, it becomes difficult to constitute a demodulator from a CMOS gate array, and LSI-ization also becomes difficult.

[0019] It aims at offering the timing regenerative circuit which realizes the phase control number of steps of a sufficiently small playback clock, realizing a high-speed timing phase level-luffing-motion property, and operating [were made in order that this invention might solve the above troubles, make over sampling technique of the data into twice a symbol rate,] on the same frequency as the twice of a symbol rate, or a symbol rate. Moreover, when performing radio by the high symbol rate of dozens of or more Mbauds, coexistence of a good bit error rate property and low-power-izing is realized, and it aims at offering the demodulator in which LSI-izing by the CMOS gate array is possible.

[0020]

[Means for Solving the Problem] the baseband phase data with which the exaggerated sample of the timing regenerative circuit concerning this invention was made into twice the symbol rate -- 1/2 symbol -- difference -- carrying out -- difference -- with phase contrast Wakebe who outputs a result as phase contrast part data ******** value ****** or the smaller one for phase contrast part absolute value data from 2pi by the phase contrast part absolute value data which carried out absolute value conversion of the phase contrast part data, and radian display as symbol frequency component data It has the symbol frequency generation section which has the data-conversion section outputted to the timing of being twice many as a symbol rate.

[0021] The multiplication section which the timing regenerative circuit concerning the next invention carries out the multiplication of the symbol frequency component outputted to symbol frequency component data from the phase control section, and is outputted as multiplication data, The low-pass filtering section which equalizes multiplication data and outputs the equalized data as a timing phase error signal, Based on a timing phase error signal, phase control of the symbol frequency component which is an output is carried out so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of a symbol frequency component as a

playback symbol clock.

[0022] The timing regenerative circuit which furthermore starts the next invention is equipped with the random walk filtering section which equalizes multiplication data in the low-pass filtering section.

[0023] The timing regenerative circuit which furthermore starts the next invention Two or more baseband phase data by which the exaggerated sample was made twice the continuous symbol rate are used. The phase data at the time of a symbol period / 4 are computed using a interpolation operation from each sampling point. Use a calculation value as phase interpolation data, and 1 / 2 symbol difference of the phase interpolation data are carried out. difference -- a result -- interpolation phase contrast part data -- carrying out -- the interpolation phase contrast part absolute value data which carried out absolute value conversion of the interpolation phase contrast part data -- Which of the value which subtracted interpolation phase contrast part absolute value data from 2pi by the radian display, or the smaller one and as symbol frequency component interpolation data The symbol frequency component interpolation data calculation section outputted to the timing of being twice many as a symbol rate, The multiplication of the inphase component of the symbol frequency outputted to symbol frequency component interpolation data from the phase control section is carried out. The complex multiplication section which carries out the multiplication of the orthogonal component of the symbol frequency which outputs as inphase multiplication data and is outputted to symbol frequency component data from the phase control section, and is outputted as rectangular multiplication data, The first integral filtering section which equalizes inphase multiplication data with the first integral mold filter, and is outputted as timing inphase data, The second integral filtering section which equalizes rectangular multiplication data with the second integral mold filter, and is outputted as timing rectangular cross data, r symbol period with timing inphase data and the arc tangent section which calculates the arc tangent value of timing rectangular cross data In quest of a timing phase error signal, it outputs from an arc tangent value. To coincidence in the first integral mold filter The integrating filter control section which outputs the integrating filter set signal which sets the vector length which timing inphase data and timing rectangular cross data show, and resets the second integral mold filter, Based on a timing phase error signal, phase control of the symbol frequency component which is an output is carried out so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock.

[0024] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. Only the time amount which can be found based on a timing phase error signal is delayed in a fixed clock, and is equipped with the clock phase shift section which outputs the signal which carried out 2 dividing of the delayed fixed clock as a playback symbol clock.

[0025] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. Only the time amount which can be found based on a timing phase error signal is delayed in a fixed clock, and is equipped with the clock phase shift section which outputs the delayed fixed clock as a playback symbol clock.

[0026] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The value which subtracted the amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with a time delay setting signal with the time delay setting signal calculation section outputted as a time delay setting signal It is the clock phase shift section which outputs the signal with which only the time amount which set up the fixed clock was delayed, and carried out 2 dividing of the delayed fixed clock as a playback symbol clock, and under [significant data receiving] setting. When the time amount to which 0 is outputted as an amendment delay value, and a time delay setting signal exceeds one period of a fixed clock during meaningless data reception is shown When the time amount to which the value equivalent to one period of a fixed clock is outputted as an amendment delay value, and a time delay setting signal exceeds -1 period of a fixed clock is shown While the value equivalent to -1 period of a fixed clock is outputted as an amendment delay value and the time delay setting signal shows the time amount of less than **one period of a fixed clock, it has the amendment delay value calculation section which outputs zero as an amendment delay value.

[0027] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The value which subtracted the amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with a time delay setting signal with the time delay setting signal calculation section outputted as a time delay setting signal It is the clock phase shift section to which only the time amount which set up the fixed clock is delayed and outputs the delayed fixed clock as a playback symbol clock, and under [significant data receiving] setting. When the time amount to which 0 is outputted as an amendment delay value, and a time delay setting signal exceeds one period of a fixed clock during meaningless data reception is shown When the time amount to which the value equivalent to one period of a fixed clock is outputted as an amendment delay value, and a time delay setting signal exceeds -1 period of a fixed clock is shown While the value equivalent to -1 period of a

fixed clock is outputted as an amendment delay value and the time delay setting signal shows the time amount of less than **one period of a fixed clock, it has the amendment delay value calculation section which outputs zero as an amendment delay value.
[0028] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The value which subtracted the amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with a time delay setting signal with the time delay setting signal calculation section outputted as first time delay setting signal The first clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as first delay clock, The value which carried out accumulation of the timing phase error signal with the second time delay setting signal calculation section outputted as second time delay setting signal, and the second time delay setting signal The second clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as second delay clock, The absolute value of the time difference of the time delay which the value of the first time delay setting signal shows, and the period of a fixed clock When smaller than the absolute value of the time difference of the time delay which the value of the second time delay setting signal shows, and the period of a fixed clock The clock change judging section which outputs the clock selection signal which specifies the second delay clock for the first delay clock when large, The clock selection section which outputs what chose one of the first delay clock and the second delay clock, and carried out 2 dividing of the clock after selection based on the clock selection signal as a playback symbol clock, At least whether the first delay clock phase is progressing or it is behind to the second delay clock, and the clock that detects and outputs detection information as a phase detecting signal A phase comparator, The equalization section which equalizes a phase detecting signal and outputs the equalized phase detecting signal, the time amount which accumulates the equalized phase detecting signal and is equivalent to this accumulation value, and the period of a fixed clock are added, and it has the error value accumulation section outputted as an amendment delay value.
[0029] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The value which subtracted the amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with a time delay setting signal with the time delay setting signal calculation section outputted as first time delay setting signal The first clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as first delay clock, The value which carried out accumulation of the timing phase error signal with the second time delay setting signal calculation section outputted as second time delay setting signal, and the second time delay setting signal The second clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as second delay clock, The absolute value of the time difference of the time delay which the value of the first time delay setting signal shows, and the period of a fixed clock When smaller than the absolute value of the time difference of the time delay which the value of the second time delay setting signal shows, and the period of a fixed clock The clock change judging section which outputs the clock selection signal which specifies the second delay clock for the first delay clock when large, The clock selection section which chooses one of the first delay clock and the second delay clock, and outputs the clock after selection as a playback symbol clock based on a clock selection signal, At least whether the first delay clock phase is progressing or it is behind to the second delay clock, and the clock that detects and outputs detection information as a phase detecting signal A phase comparator, The equalization section which equalizes a phase detecting signal and outputs the equalized phase detecting signal, the time amount which accumulates the equalized phase detecting signal and is equivalent to this accumulation value, and the period of a fixed clock are added, and it has the error value accumulation section outputted as an amendment delay value.
[0030] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. A fixed clock pi phase shift by radian display the signal carried out with a clock selection signal with pi phase shift section outputted as a pi phase shift clock One of a fixed clock and the pi phase shift clocks is made into the clock for a comparison. The clock change section which uses another side as the clock for phase shifts, and outputs it, respectively, The surplus value at the time of carrying out accumulation of the timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a fixed clock with a time delay setting signal with the accumulation section outputted as a time delay setting signal The clock phase shift section which outputs the signal with which only the time amount which set up the clock for phase shifts was delayed, used the delayed signal as the playback clock, and carried out 2 dividing of the playback clock as a playback symbol clock, The first 2-minute periphery which carries out 2 dividing of the clock for a comparison, and outputs the clock which carried out 2 dividing as a 2 dividing clock for a comparison, The second 2-minute periphery which carries out 2 dividing of the playback clock, and outputs the clock which carried out 2 dividing as a playback 2 dividing clock, When 2 dividing clock for a comparison is sampled with a playback 2 dividing clock and change produces it to the sampled data It has the clock change signal output part which outputs the reset signal which it is at the change time and resets the accumulation value of accumulation circles to 0, and the clock selection signal with which it is at the change time, and logic "1" and logic "0" change.
[0031] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the

transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. A fixed clock pi phase shift by radian display the signal carried out with a clock selection signal with pi phase shift section outputted as a pi phase shift clock One of a fixed clock and the pi phase shift clocks is made into the clock for a comparison. The clock change section which uses another side as the clock for phase shifts, and outputs it, respectively, The surplus value at the time of carrying out accumulation of the timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a fixed clock with a time delay setting signal with the accumulation section outputted as a time delay setting signal The clock phase shift section to which only the time amount which set up the clock for phase shifts is delayed, uses the delayed signal as a playback clock, and outputs a playback clock as a playback symbol clock, The first 2-minute periphery which carries out 2 dividing of the clock for a comparison, and outputs the clock which carried out 2 dividing as a 2 dividing clock for a comparison, The second 2-minute periphery which carries out 2 dividing of the playback clock, and outputs the clock which carried out 2 dividing as a playback 2 dividing clock, When 2 dividing clock for a comparison is sampled with a playback 2 dividing clock and change produces it to the sampled data It has the clock change signal output part which outputs the reset signal which it is at the change time and resets the accumulation value of accumulation circles to 0, and the clock selection signal with which it is at the change time, and logic "1" and logic "0" change.

[0032] The timing regenerative circuit which furthermore starts the next invention In the clock phase shift section a fixed clock from time amount y to time amount yx (N-1) It delays by y time step and the delay clock of an individual (N-1) is generated. A fixed clock, The delay clock group generation section which outputs the clock of N individual containing the delay clock of an individual as a delay clock group, (N-1) The clock selection-signal generation section which generates and outputs a clock selection signal based on a time delay setting signal, it is ******** (N-1) about the delay section which chooses one from a delay clock group, is equipped with the clock selection section outputted as a delay clock based on a clock selection signal, and gives a time delay y by the delay element in the delay clock group generation section further.

[0033] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The accumulation section which outputs the surplus value at the time of carrying out accumulation of the timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a local sine wave as a time delay setting signal, The cosine value at the time of writing the value which a time delay setting signal shows with the phase to the period of a local sine wave, The cosine sign transducer which calculates a sign value and is outputted as cosine data and sign data, respectively, Quadrature modulation of cosine data and the sign data is carried out by the local sine wave. The quadrature modulation section which outputs the signal by which quadrature modulation was carried out as a timing regenerative signal and which consists of two DA converters, two low pass filters, two multipliers, one adder, and one pi/2 phase shifter, It has the hard decision section to output by using as a playback symbol clock the signal which carried out the hard decision of the timing regenerative signal, and carried out 2 dividing of the data after a hard decision.

[0034] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The accumulation section which outputs the surplus value at the time of carrying out accumulation of the timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a local sine wave as a time delay setting signal, The cosine value at the time of writing the value which a time delay setting signal shows with the phase to the period of a local sine wave, The cosine sign transducer which calculates a sign value and is outputted as cosine data and sign data, respectively, Quadrature modulation of cosine data and the sign data is carried out by the local sine wave. The quadrature modulation section which outputs the signal by which quadrature modulation was carried out as a timing regenerative signal and which consists of two DA converters, two low pass filters, two multipliers, one adder, and one pi/2 phase shifter, The hard decision of the timing regenerative signal is carried out, and it has the hard decision section which outputs the data after a hard decision as a playback symbol clock.

[0035] The timing regenerative circuit which furthermore starts the next invention Based on a timing phase contrast signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and have the phase control section which outputs the most significant bit of a symbol frequency component as a playback symbol clock, and it sets in the phase control section further. The accumulation section which outputs the surplus value at the time of carrying out accumulation of the timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a fixed clock as a time delay setting signal, The cosine value at the time of writing the value which a time delay setting signal shows with the phase to the period of a fixed clock, The cosine sign transducer which calculates a sign value and is outputted as cosine data and sign data, respectively, 2 dividing of the 2 double fixed clock which has a clock twice the frequency of playback is carried out. The first sign pars inflexa which outputs cosine data as it is when the 2-minute periphery which generates a fixed clock, and the logic of a fixed clock are "1", carries out the multiplication of "-1" to cosine data, and outputs it to them when the logic of a fixed clock is "0", The second sign pars inflexa which outputs sign data as it is when the logic of a fixed clock is "1", carries out the multiplication of "-1" to sign data, and outputs it to them when the logic of a fixed clock is "0", When a 2 double fixed clock is logic "1", the output value of the first sign pars

inflexa is outputted as playback timing data 4 times. The clock amplitude value selection section which outputs the output value of the second sign pars inflexa as timing playback data 4 times when a 2 double fixed clock is logic "0", The DA translation section which carries out the DA translation of the timing playback data 4 times, and is changed into an analog timing signal, The analog low-pass filtering section which outputs the signal which carried out low-pass filtering of the analog timing signal, and removed harmonic content as a timing regenerative signal, The hard decision of the timing regenerative signal is carried out, and it has the hard decision section which outputs the data after a hard decision as a playback symbol clock.

[0036] The timing regenerative circuit which the demodulator furthermore applied to the next invention considered the baseband phase data by which the exaggerated sample was made twice the symbol rate as the input, and carried out phase simulation to the transmission timing of a transmitting side and which outputs a playback symbol clock, The receiving IF signal by which the PSK modulation was carried out to the receiving IF signal by which amplitude limiting was carried out to the amplitude-limiting section which carries out amplitude limiting Carry out complex multiplication of the local signal which has the same frequency as an IF signal, and low-pass filtering of the inphase component after complex multiplication and the orthogonal component after complex multiplication is carried out. The rectangular detection section outputted as a baseband inphase signal and a baseband rectangular cross signal, respectively, The exaggerated sample of a baseband inphase signal and the baseband rectangular cross signal is carried out to the timing of being twice many as the symbol rate which synchronized with the playback symbol clock., respectively Baseband inphase data, The sampling section outputted as baseband rectangular cross data, and baseband inphase data, With a playback symbol clock with the polar-coordinate transducer which carries out polar-coordinate conversion of the baseband rectangular cross data, and outputs the data after polar-coordinate conversion as baseband phase data Baseband phase data are latched and it has the data judging section which judges and outputs recovery data from the phase data after a latch.

[0037] The demodulator furthermore applied to the next invention outputs the playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side. The timing regenerative circuit which generates a playback symbol clock from a fixed clock twice the frequency of a symbol rate, or a local sine wave twice the frequency of a symbol rate, The receiving IF signal by which the PSK modulation was carried out to the receiving IF signal by which amplitude limiting was carried out to the amplitude-limiting section which carries out amplitude limiting Carry out complex multiplication of the local signal which has the same frequency as an IF signal, and low-pass filtering of the inphase component after complex multiplication and the orthogonal component after complex multiplication is carried out. The rectangular detection section outputted as a baseband inphase signal and a baseband rectangular cross signal, respectively, A baseband inphase signal and a baseband rectangular cross signal are sampled with a playback clock., respectively Baseband inphase data, The sampling section outputted as baseband rectangular cross data, and baseband inphase data, With a playback symbol clock with the polar-coordinate transducer which carries out polar-coordinate conversion of the baseband rectangular cross data, and outputs the data after polar-coordinate conversion as baseband phase data Baseband phase data are latched and it has the data judging section which judges and outputs recovery data from the phase data after a latch.

[0038] The demodulator furthermore applied to the next invention outputs the playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side. The timing regenerative circuit which generates a playback symbol clock from the same fixed clock of a frequency as a symbol rate, or the local sine wave of the same frequency as a symbol rate, The receiving IF signal by which the PSK modulation was carried out to the receiving IF signal by which amplitude limiting was carried out to the amplitude-limiting section which carries out amplitude limiting Carry out complex multiplication of the local signal which has the same frequency as an IF signal, and low-pass filtering of the inphase component after complex multiplication and the orthogonal component after complex multiplication is carried out. The rectangular detection section outputted as a baseband inphase signal and a baseband rectangular cross signal, respectively, A baseband inphase signal and a baseband rectangular cross signal are sampled in the standup and falling of a playback symbol clock., respectively Baseband inphase data, The sampling section outputted as baseband rectangular cross data, and baseband inphase data, With a playback symbol clock with the polar-coordinate transducer which carries out polar-coordinate conversion of the baseband rectangular cross data, and outputs the data after polar-coordinate conversion as baseband phase data Baseband phase data are latched and it has the data judging section which judges and outputs recovery data from the phase data after a latch.

[0039]

[Embodiment of the Invention]

gestalt 1. of operation -- with the gestalt 1 of implementation of this invention, a symbol rate explains the demodulator for TDMA (Time Division Multiple Access) communication system which performs the high-speed radio transmission of 50Mbaud(s). A demodulator receives the IF signal by which the QPSK modulation was carried out, and restores to data. Moreover, the timing regenerative circuit in a demodulator uses a twice as many fixed clock as a symbol rate as a clock of operation, and reproduces the playback symbol clock which synchronized with receiving timing using the BTR pattern in each burst head.

[0040] Drawing 1 is drawing showing the configuration of the demodulator containing timing regenerative-circuit 7A by the gestalt 1 of operation. 21a and 21b are a mixer and a fixed clock generator for timing playback a timing regenerative circuit and whose 8A of a low pass filter and 7A pi/2 phase shifter, and 23a and 23b are twice the frequencies of a symbol rate (the same frequency as a bit rate) for 22 among drawing. In addition, the same agreement is given to the part equivalent to the conventional technique. Moreover, drawing 3 shows the configuration of timing regenerative-circuit 7A of the gestalt 1 of operation. inside of drawing, and 71A -- the symbol frequency component generation section and 711A -- phase contrast Wakebe and 72A -- the multiplication section and 72f -- for a random walk filter and 74A, as for the playback symbol clock generation section and 76, the phase control section and 75 are [a D flip-flop and 73A / the low-pass filtering section and 73e / the memory for topology and 77] filter information memory. Moreover, drawing 5 is drawing showing the configuration of phase control section 74A in the

'timing regenerative circuit of drawing 3 . For 741, the time delay setting signal calculation section and 743 are [an adder and 741c of the clock phase shift section and 741a] D flip-flops among drawing. Moreover, drawing 6 shows another phase control section corresponding to phase control section 74A of drawing 5 , and shows the configuration of phase control section 74A which has the function to avoid malfunction produced according to the delay error of a delay element. For 741A, the time delay setting signal calculation section and 742 are [the clock phase shift section and 741b of the amendment delay value calculation section and 743A] subtractors among drawing. Moreover, drawing 7 shows the configuration of the clock phase shift section 743 of the gestalt 1 of this operation. The clock selection-signal generation section and 7432 among drawing 7431 The delay clock group generation section, The clock selection section, and 7432a, 7432b, 7432c, 7432d and 7432e 7433 A delay element, 7432f, 7432g, 7432h, 7432i, 7432j, and 7432k A buffer, 7433a, 7433b, 7433c, 7433d, 7433e, and 7433f are [an AND gate and 7433m of a D flip-flop and 7433g, 7433h, 7433i, 7433j, 7433k, and 7433l.] OR gates.

[0041] Next, actuation of the demodulator of the gestalt 1 of this operation is explained. First, whole actuation is explained with reference to drawing 1 . Like the conventional example, amplitude limiting of the IF signal by which the QPSK modulation was carried out is carried out by the limiter 1, and it is inputted into the rectangular detector circuit 2. Using the same local signal as the center frequency of an IF signal from the local oscillator 3 for rectangular detection, like the conventional example, rectangular detection is performed to the IF signal by which amplitude limiting was carried out, and a baseband inphase signal and a baseband rectangular cross signal are acquired in the rectangular detector circuit 2. The rectangular detector circuit 2 carries out the multiplication of the IF signal by which amplitude limiting was carried out, and the local signal for rectangular detection by mixer 21a, removes harmonic content by low pass filter 23a, it outputs a baseband inphase signal, carries out the multiplication of the local signal for rectangular detection which carried out pi / 2 phase shifts with pi/2 phase shifter 22, and the IF signal by which amplitude limiting was carried out by mixer 21b, removes harmonic content by low pass filter 23b, and outputs a baseband rectangular cross signal.

[0042] In the conventional example, although the baseband inphase signal and the baseband rectangular cross signal were sampled using playback 4 clock-doubling 4 times the frequency of a symbol rate, the sampling section 4 in the gestalt 1 of this operation samples a baseband inphase signal and a baseband rectangular cross signal using playback 2 clock-doubling twice the frequency of a symbol rate, and outputs the 2 double exaggerated sample data after an AD translation as baseband inphase data and baseband rectangular cross data. The polar-coordinate conversion circuit 5 carries out polar-coordinate conversion of the baseband inphase data and baseband rectangular cross data by which the exaggerated sample was made twice this symbol rate, and outputs the data after polar-coordinate conversion as baseband phase data. The data judging circuit 6 performs differentially coherent detection using the phase data of the nyquist point of having extracted and extracted the phase data of a nyquist point from the baseband phase data obtained to the timing of being twice many as a symbol rate using the playback symbol clock, and outputs recovery data. Using the baseband phase data from the sampling circuit 4 obtained to the timing of being twice many as a symbol rate, timing regenerative-circuit 7A performs phase control of playback 2 clock-doubling so that the nyquist point of a baseband inphase and a rectangular signal may be sampled, and it performs phase control of a playback symbol clock so that the phase data of a nyquist point may be extracted in the data judging circuit 6. Moreover, timing regenerative-circuit 7A operates with a fixed clock twice the frequency of the symbol rate outputted from fixed clock generator 8for timing playback A, and performs clock phase control at intervals of an about 1-/16 symbol step.

[0043] Next, actuation of timing regenerative-circuit 7A of the gestalt 1 of this operation is explained based on drawing 3 . Symbol frequency component generation section 71A generates data sequence deltatheta (iT/2) which is the timing of being twice many as a symbol rate, and contains a symbol frequency component from the baseband phase data theta (iT/2) by which the exaggerated sample was made twice the symbol rate by the following formulas (8). However, it is i= {1, 2, 3, --}.

deltatheta(iT/2) =min {|theta(iT/2)-theta(i-1) (T/2) | and 2pi-|theta(iT/2)-theta(i-1) (T/2) |} (8)

Symbol frequency component generation section 71A consists of phase contrast part circuit 711A and data-conversion circuit 712B, and phase contrast part circuit 711A performs difference of theta(iT/2)-theta (i-1) (T/2) of a formula (8). This processing is realizable in the easy circuit which carries out difference of the phase data delayed by 1 sampling-time D-flip-flop 711a from current phase data using subtractor 711c. Moreover, in the data-conversion circuit 712, like the conventional method, processing of the above-mentioned formula (8) is realized by absolute value conversion circuit 712a and phase data-conversion circuit 712b, and data sequence deltatheta (iT/2) containing a symbol frequency component is obtained.

[0044] Multiplication section 72A asks for multiplication value [for one symbol] M (jT) of deltatheta (iT/2) containing the frequency component fs of this transmitting side, and the symbol frequency by the side of a receiver (fs**) by the following formulas (9). M (jT) is a multiplication value in j (= 1, 2, 3, --) symbol eye.

[0045]

[Equation 3]

$$M(jT) = \sum_{i=2j-1}^{2j} \Delta\theta(iT/2) \times \cos 2\pi fs'(iT/2) \qquad (9)$$

[0046] the above-mentioned cos2pifs** (iT/2) - 1, 1, and - 1, 1, -- Since it is a repeat, it can ask for the above-mentioned M (jT) easily by the following formulas (10).

M(jT) =deltatheta(2jT/2)-deltatheta (2j-1) (T/2) (10)

M (jT) subtracts current deltatheta (iT/2) by subtractor 72c, and is easily obtained from deltatheta (iT/2) latched by D-flip-flop 72a which operates in the start of playback 2 clock-doubling by latching the data after subtraction by 72f of D flip-flops which

operate in the start of a playback symbol clock.

[0047] If this M (jT) is equalized, it can distinguish whether the phase of the symbol timing of a receiving side is progressing, or it is behind. Hereafter, this is explained. Considering only symbol frequency component sin2pifs(t)+A contained in deltatheta (t), 1/of processings currently performed by D-flip-flop72a and subtractor 72c is difference 2 symbol. this difference -- as shown in the following formulas (11), the symbol frequency component from which the offset A of 2sin (2pifs (t)) was removed is contained in value Q (t).

Q (t) = (sin2pifs (t) +A)
- sin(2pifs (t-T/2)) +A
= sin2pifs (t) +A
- sin2pifs(t)-pi+A
= sin2pifs (t) +A
- -sin2pifs (t) +A
= 2sin (2pifs (t)) (11)

What sampled this Q (t) to the symbol frequency timing of a receiving side is set to M (jT). When Q (t) is sampled to the timing of time amount t=jT (j= 1, 2 and 3, --, T; symbol period), the average of M (jT) is set to 0. Moreover, when Q (t) is sampled to the timing of time amount jT<t<3jT/2, the average of M (jT) shows a forward value, and when Q (t) is sampled to the timing of time amount 3jT/2<t<2jT, the average of M (jT) shows a negative value. Therefore, if the positive/negative of equalized M (jT) is judged, it can judge whether the timing phase is progressing or it is behind.

[0048] Actuation of Q (t) and timing regenerative-circuit 7A of the gestalt 1 of this operation is shown in drawing 8 . Drawing 8 is an example of the phase data of a random pattern, and phase data and ** of a dotted line are nyquist points among drawing. With the gestalt of this operation, since a modulation technique is a QPSK modulation technique, phase fluctuation of each nyquist point is set to **90 (degree), and 180 (degree) and 0 (degree). Q (t) generated from the phase data of this random pattern is shown by the continuous line of drawing 8 . When the initial phase of a playback symbol clock is progressing from the nyquist point location as shown in the timing of an upper case so that clearly from drawing, Q (t) sampled in the playback symbol clock start and (= M(jT)) are "forward." Moreover, as the initial phase of a playback symbol clock shows the timing of the lower berth, when it is from the nyquist point location behind, Q (t) sampled in the playback symbol clock start and (= M(jT)) are "negative." It turns out that the absolute value of this data of Q (t) becomes large in the place where phase fluctuation of baseband phase data is large. Therefore, this timing regenerative-circuit 7A can perform high-speed drawing in to a fixed pattern whose fluctuation of baseband phase data is large.

[0049] Next, low-pass filtering section 73A equalizes this M (jT), and outputs M after equalization (jT) as a timing phase error signal. With the gestalt of this operation, it equalizes using random walk filter 73e, and the UPj signal to which a phase is advanced, and the DWj signal which delays a phase are outputted as a timing phase error signal. An example of the flow of random walk filter 73e of operation is shown in drawing 9 . Random walk filter 73e consists of an updown counter and a comparator. If the value of an updown counter is set to Rj (j= 1, 2 and 3, --), actuation will be started from beginning Rj=0. Moreover, as shown in a formula (12), what judged M (jT) by -1, and {0, 1} for every symbol is inputted into the flow of drawing 9 of operation as LEADj.

LEADj= 1 (M(jT)<0)
LEADj=-1 (M(jT)>0)
LEADj= 0 (M(jT)=0)
(12)

If Rj is set to -N in the UPj signal of the logic "0" to which a clock phase will be advanced if random walk filter 73e continues actuation and Rj is set to N as shown in the flow of drawing 9 of operation, the DWj signal of the logic "0" which delays a clock phase will be outputted, respectively. After one of signal outputs, Rj is reset by "0" and the condition of 1 symbol time amount Rj=0 is maintained. Moreover, when Rj is in the range of (-N<Rj<N), UPj of logic "1" which does not give a phase control instruction, and DWj of logic "1" are outputted. The band of a random walk filter can be found by the filter constant N so that drawing 9 may also show. Therefore, what is necessary is to set up N small to perform high-speed level luffing motion, and just to set up N greatly to realize the low jitter of the phase after drawing in. Although the case where a random walk filter was used for low-pass filtering section 73A was taken up with the gestalt of this operation, also except the above-mentioned random walk filter 73e, a moving-average circuit, an infinity impulse response circuit, etc. equalize M (jT), and low-pass filtering section 73A should just remove a noise component etc.

[0050] Next, actuation of phase control section 74A is explained. Like the conventional phase control section 74, phase control section 74A is about 1/16 sufficiently fine phase control spacing of a symbol period, and controls the phase of playback 2 clock-doubling twice the frequency of a symbol rate. if, as for phase control section 74A, a symbol period will advance the phase of playback 2 clock-doubling about 1/16 if the UPj signal of logic "0" is inputted, and the DWj signal of logic "0" is inputted -- the phase of playback 2 clock-doubling -- 1/of a symbol period -- it delays about 16. However, the point that phase control section 74A differs from the conventional phase control section 74 is a point which considers a fixed clock twice the frequency of a symbol rate as an input (the conventional phase control section 74 needed the clock 16 times the frequency of a symbol rate). Drawing 5 is used for below and actuation of phase control section 74A is explained to it. First, the time delay setting signal calculation circuit 741 accumulates a timing phase error signal during significant data reception of a burst signal. With the gestalt of this operation, if the UPj signal of logic "1" is inputted and "-1" will be inputted into the DWj signal of logic "1", "1" will be inputted into the time delay setting signal calculation circuit 741 as a timing phase error value Ej, respectively. If the circuit of the

time delay setting signal calculation circuit 741 is constituted from a m-bit data bus, the time delay setting signal Kj which is time delay setting signal calculation circuit 741 output can be found by the following formulas (13).

Kj= mod(Kj-1+Ej,2m) (13)

m will be taken as the value with which the following formulas (14) are filled, if phase control spacing of a playback clock is made into T/Z (T; symbol period).

m=log2(Z/2) (14)

In this case, in order to design by Z= 16, m is taken as the value "3" with which a formula (14) is filled. Therefore, if the UPj signal of logic "1" continues being inputted during significant data reception when referred to as m= 3, Kj will change with 7, 6, 5, --, 1, 0, 7 and 6, and --. On the contrary, if the DWj signal of logic "1" continues being inputted, Kj will change with 7, 0, 1, 2, --6, 7, 0 and 1, and 2 --. Kj which takes this value of 0-7 is inputted into the clock phase shift section 743.

[0051] Next, actuation of the clock phase shift section 743 is explained using drawing 7 . First, the delay clock group generation circuit 7432 generates the clock with which the phases of eight pieces differ from a fixed clock twice the frequency of a symbol rate. The frequency of each eight clock is twice the symbol rate. Moreover, as shown in drawing 7 , each clock connects to a seven-piece serial the delay element which gives delay of T / 16 symbol time amount, and amplifies and generates with a buffer the output clock of each delay element, and the fixed clock which is an input, respectively. The clock selection-signal generation circuit 7431 generates the 8-bit clock selection signal Sj from the time delay setting signal Kj by the following formulas (15).

Sj=2Kj+2Kj-1 (15)

The clock selection circuitry 7433 chooses and outputs one from the eight above-mentioned clocks with the clock selection signal Sj. The clock selection section 7433 consists of circuits shown in drawing 7 so that the phase of an output clock may not be confused at the time of a clock selection-signal Sj change. As shown in drawing 7 , retiming of the bit [d-th] data (however, 1<=d<=2m) is carried out from the low order of the clock selection signal Sj in falling of the fixed clock which passed the delay element of an individual (d-1), and the AND of each of this signal by which retiming was carried out, and each clock which carried out retiming of it is searched for in each AND gate. Furthermore, playback 2 clock-doubling is obtained by searching for the OR of each AND-gate output by the OR gate.

[0052] A timing chart shows the example of the clock phase-shifting circuit 743 of operation in case UP signal of logic "1" occurs in drawing 10 and Kj changes from "3" to it "2." What delayed the clock with which that to which the clock outputted from buffer 7432f amplified the input fixed clock with the buffer, and the clock outputted from buffer 7432g are outputted from buffer 7432f T/16 by delay element 7432a, and the clock outputted from buffer 7432h delay the clock outputted from buffer 7432g T/16 by delay element 7432b. Since "-1" is inputted into the time delay setting circuit 741 in the condition that Kj is "3" when a UPj signal shows logic "0" by symbol period width of face as shown in drawing 10 , Kj changes to "2" from "3." At this time, Sj is the timing shown in drawing 10 , and changes with formulas (15) with "8"->"12"-> "4." In order to carry out retiming of each of this bit of Sj in the eight above-mentioned clock fallings, respectively, the output of the signal by which retiming was carried out in falling of the clock outputted from buffer 7432g, i.e., register 7433b, serves as timing shown in drawing 10 . Moreover, the output of the signal by which retiming was carried out in falling of the clock outputted from buffer 7432h, i.e., register 7433b, serves as timing shown in drawing 10 . All the signals outputted from other registers serve as logic "0" (not shown). Therefore, the output of AND7433h and the output of AND7433i serve as timing shown in drawing 10 , and all other AND outputs serve as logic "0" (not shown [the output of logic"0"]). Playback 2 clock-doubling is carried forward T/16 (symbol), without confusing a start point, as shown in drawing 10 , in order to take the OR of these AND [all] outputs. Like the timing shown in drawing 11 , if a clock is chosen without performing each above-mentioned processing, in case the phase of playback 2 clock-doubling is delayed, a phase may be confused by the clock change over point, and, thereby, a cycle slip of a clock will arise. Even when performing each above-mentioned actuation, and Kj was asynchronous, and changes to the eight above-mentioned fixed clocks each or it changes to "7" from "7" to "0", or "0", the phase of an output clock cannot be confused and control of the playback 2 clock-doubling phase according to change of Kj can be ensured.

[0053] From the input fixed clock of Kj and the playback 2 clock-doubling outputted from the clock selection circuitry 7433 to phase contrast deltap (radian), the following formulas (16a) are materialized from the above thing.

delta p=pixKj / 2 (16a) (m-1)

With the gestalt of this operation, the symbol rate is set to 50Mbaud(s), and since clock phase control spacing is 1/16 of the symbol period T, the amount of delay of each delay element which constitutes the delay clock group generation circuit 7432 of drawing 7 has the need of making it 1/(16x50x106) (second) =1.25 (n-second).

[0054] However, with temperature etc., the time delay of this delay element may shift from the set point, and can consider the case where it malfunctions, with the configuration of the phase control section shown in drawing 5 in that case. If error time amount of the amount of delay of this one delay element is set to alpha, the following formulas (17a) will be materialized from the input fixed clock of Kj and the playback 2 clock-doubling outputted from the clock selection circuitry 7433 to phase contrast deltap (radian).

deltap=mod (pi / 2(m-1)+4alpha pi/T) (xKj, 2pi)

(17a)

The Kj pair deltap property at the time of making alpha into a parameter for an example at drawing 12 is shown. It turns out that malfunction arises in phase control as the absolute value of alpha becomes large. For example, in order to delay a phase, the case where Kj makes it change with 6, 7, 0, 1, 2, and -- is considered. As for deltap, in the case of alpha= 0, a phase is late by T/16 of regular intervals with 1.5pi, 1.75pi, 0, 0.25pi, 0.5pi, and --. However, when, as for deltap, Kj changes to "0" from "7" with 1.98pi, 0.31pi, 0, 0.33pi, 0.66pi, and -- in the case of alpha=1/50, a phase will progress to 0 from 0.31pi. Moreover, conversely, deltap will be from 1.19pi in a phase rapidly to 0, when Kj changes to "0" from "7" with 1.02pi, 1.19pi, 0, 0.17pi, 0.34pi, and -- in the

case of alpha=-1/50. Thus, although the phase control section of drawing 5 is effective when it can realize by very easy circuitry and the absolute value of alpha shows a small value which turbulence does not produce in phase control actuation When the absolute value of alpha is large, in case Kj changes to "0" rapidly from "0" to "2m-1", or "2m-1", turbulence will arise in phase control actuation and a timing phase jitter will increase.

[0055] Thus, when the absolute value of alpha is large, it considers as a configuration as shows phase control section 74A to drawing 6 . However, the phase control section of drawing 6 is effective only when a meaningless signal (for example, the signal of only a noise component, a preamble pattern signal) exists between significant burst signals with TDMA communication system like the gestalt of this operation. Henceforth, the phase control section of drawing 6 is explained. In the phase control section of drawing 6 , in the case of alpha= 0, in a formula (17), the abrupt change of the value of Kj used as the cause which turbulence produces in phase control actuation during significant burst signal reception paying attention to deltap of Kj and deltap of Kj**8 being in agreement is not given, but the abrupt change to Kj-> (Kj**8) is given at the time of meaningless signal reception. This realizes stable phase control actuation during significant burst signal reception. Henceforth, each actuation is explained.

[0056] First, time delay setting signal calculation circuit 741A subtracts the value of the amendment delay value calculation circuit 742 from the value which accumulated the timing phase error signal during significant data reception of a burst signal, and was accumulated during meaningless data reception of a burst signal. If the circuit of the time delay setting signal calculation circuit 741 is constituted and the value of the amendment delay value calculation circuit 742 is set to Hj with the data bus of n (= m+1) bit, the time delay setting signal Kj which is a time delay setting signal calculation circuit 741A output can be found by the following formulas (18).

Kj= mod(Kj-1+Ej-Hj,2n) (18)

If phase control spacing of a playback clock is made into T/Z (T; symbol period), let the value of n be the value with which the following formulas (19) are filled.

n>=log2Z (19)

In this case, in order to design by Z= 16, n is taken as the value "4" with which a formula (19) is filled. Hj always outputs "0" during significant data reception of a burst signal. Therefore, if the UPj signal of logic "1" continues being inputted during significant data reception when referred to as m= 4, Kj will change with 15, 14, 13, --, 1, 0, 15 and 14, and --. On the contrary, if the DWj signal of logic "1" continues being inputted, Kj will change with 15, 0, 1, 2, --14, 15, 0 and 1, and 2 --. Kj which takes this value of 0-15 is inputted into clock phase-shifting circuit 743A.

[0057] Clock phase-shifting circuit 743A is easily realizable by the same circuitry fundamentally with the clock phase-shifting circuit 743 of drawing 7 . That is, by the formula (15), the clock selection-signal generation circuit 7431 (drawing 7) generates the 16-bit clock selection signal Sj from the time delay setting signal Kj, it generates 16 clocks from 16 delay elements to which series connection of the delay clock group generation circuit 7432 was carried out, and the clock selection circuitry 7433 chooses one from 16 clocks. The clock selection circuitry 7433 which chooses one from 16 clocks Retiming of the bit [d-th] data (however, 1<=d<=16) is carried out from the low order of the clock selection signal Sj in falling of the fixed clock which passed the delay element of an individual (d-1). Each of this signal by which retiming was carried out, An AND with each clock which carried out retiming of it is searched for in the 16 AND gates each, and the OR of the AND-gate output of 16 pieces each is further searched for by the OR gate. If Kj counts up from the above thing to 0, 1, 2, --14, and 15 and 0 in the case of alpha= 0, the phase from the fixed clock of playback 2 clock-doubling will become what (namely, it rotates two times) is changed from 0 to 4pi.

[0058] Next, with a burst gate signal, the amendment delay value calculation circuit 742 starts actuation at the time of meaningless signal reception, and performs processing of the following formulas (20) to Kj to certain threshold epsilon (<=4).

Kj<- Kj+2n-1 (Kj<=epsilon)

Kj<- Kj-2n-1 (Kj>=15-epsilon)

Kj<- Kj (epsilon<Kj <15-epsilon) (20)

That is, in the case of n= 4, the amendment delay value calculation circuit 742 outputs Hj which is an output value by the following formulas (21) at the time of meaningless signal reception, is giving subtractor 741b in time delay setting signal calculation circuit 741A, and realizes processing of a formula (20).

Hj=-8 (Kj<=epsilon)

Hj=+8 (Kj>=15-epsilon)

Hj= 0 (epsilon<Kj <15-epsilon) (21)

The above-mentioned phase control section has the effective fluctuation range of Kj at the time of burst signal reception to below "8" (when it is made time amount, it is T/2 or less). What is necessary is just to design the value of n so that a formula (22) may be filled when the amount range of fluctuation of Kj at the time of burst signal reception is q> 8.

n>=log2 (2q) (22)

Next, to drawing 3 , return and the playback symbol clock generation circuit 75 carry out 2 dividing of the playback 2 clock-doubling outputted from phase control section 74A, and generate a playback symbol clock here.

[0059] When the initial phase of a playback symbol clock is progressing from the nyquist point as shown in the upper case of drawing 8 if a series of actuation so far is explained using drawing 8 , since Q (t) sampled in the playback symbol clock start and (= M(jT)) are "forward", LEADj=-1 is inputted into random walk filter 73e. Random walk filter 73e equalizes this, the DWj signal of the logic "1" which delays a phase is outputted, and phase control section 74A delays the phase of playback 2 clock-doubling with the DWj signal of this logic "1." In the playback symbol clock generation section 75, since a playback symbol clock carries out 2 dividing of the playback 2 clock-doubling and is generated, it is behind [coincidence] also in the phase of a

playback symbol clock. After a number - dozens symbols, the location of the start point of a playback symbol clock and a nyquist point is in agreement with this the actuation of a series of (for example, it is shown in drawing 8 like). Moreover, as the initial phase of a playback symbol clock shows the lower berth of drawing 8 , when it is behind the nyquist point, since Q (t) sampled in the playback symbol clock start and (= M(jT)) are "negative", LEADj=1 is inputted into random walk filter 73e. Random walk filter 73e equalizes this, the UPj signal of the logic "1" to which a phase is advanced is outputted, and phase control section 74A advances the phase of playback 2 clock-doubling with the UPj signal of this logic "1." Since a playback symbol clock carries out 2 dividing of the playback 2 clock-doubling and is generated in the playback symbol clock generation section 75, the phase of a playback symbol clock also progresses to coincidence. After a number - dozens symbols, the location of the start point of a playback symbol clock and a nyquist point is in agreement with this the actuation of a series of (for example, it is shown in drawing 8 like).

[0060] If topology and filter information are saved at the tail of a burst and such information is loaded at the next burst head at the time of burst signal reception, it is not necessary to draw timing regenerative-circuit 7A for every burst signal, and actuation will be stabilized further. In this case, based on the timing of a burst gate signal, the memory 76 for topology saves Kj value of phase control section 74A at the tail of a burst, and phase control section 74A is the next burst head, and it loads Kj of the memory 76 for topology. Moreover, based on the timing of a burst gate signal, the memory 77 for filter information saves Rj value in random walk filter 73e at the tail of a burst, and random walk filter 73e is the next burst head, and it loads Rj of the memory 77 for filter information. In addition, although the phase control number of steps was made into 1/16 of the symbol periods T with the gestalt 1 of this operation, the phase control number of steps should just be the sufficiently small value of the T/Z symbol step which fills Z>=16.

[0061] Thus, since it operates like [the demodulator shown in the gestalt 1 of this operation] the conventional example using the receiving PSK signal by which amplitude limiting was carried out, it can constitute from an easy circuit which has a limiter in the preceding paragraph, and the miniaturization of a circuit can be realized. Moreover, since the demodulator shown in the gestalt 1 of this operation is the configuration of the feedback mold which performs an AD translation to the timing of playback 2 clock-doubling, it can operate by the twice of the symbol rate which is the sampling rate of the one half of the conventional example, and can realize low-power-ization. Furthermore, the conventional timing regenerative circuit 7 inputs a x times as many fixed clock as a symbol rate. Timing regenerative-circuit 7A shown in the gestalt 1 of this operation to having performed 1/x of a symbol period of phase control steps A twice as many fixed clock as a symbol rate is inputted, to a symbol period, it is stabilized and sufficiently small phase control step spacing (1/16 or less [of a symbol period]) is realized. Therefore, especially, when symbol rates, such as a high-speed radio-transmission system, are high, timing regenerative-circuit 7A can realize low-power-ization, and becomes easy [a circuit design]. Moreover, timing regenerative-circuit 7A can perform high-speed drawing in to a data pattern especially with large phase fluctuation by symbol frequency generation section 71A using the baseband phase data by which the exaggerated sample was carried out by the twice of a symbol rate.

[0062] Gestalt 2. drawing 2 of operation is drawing showing the configuration of the demodulator of the gestalt 2 of operation, and operates the clock of a timing regenerative circuit of operation on the frequency of a symbol rate. For an A-D converter and 4e, in drawing, an inverter and 5a are [4A / a sampling circuit and 4c and 4d / a timing regenerative circuit and 8B of a polar-coordinate conversion circuit and 7B] the fixed clock generators of the frequency of a symbol rate. Moreover, drawing 4 is the block diagram of the timing regenerative circuit in the gestalt 2 of this operation, and, for the multiplication section and 73A, the low-pass filtering section and 74B of the phase control section and 76 are [71B / the symbol frequency component generation section and 72B / the memory for topology and 77] the memory for filter information. Symbol frequency generation section 71B consists of phase contrast part circuit 711B and data-conversion circuits 712A and 712B further. And for a D flip-flop and 711f and 711g, a subtractor and 711h are [711d and 711e / a subtractor and 72f of an inverter and 72c] D flip-flops.

[0063] Although two A-D converters sampled in the start of playback 2 clock-doubling constituted the sampling circuit 4 from the gestalt 1 of operation, twice as many over sampling technique as a symbol rate is realized with the gestalt 2 of operation as a configuration of sampling circuit 4A constituted from two A-D converters 4a and 4b sampled in the start of a playback symbol clock as shown in drawing 2 , and two A-D converters 4c and 4d sampled in falling. In falling, a sampling action is realizable, if the playback symbol clock which inverter 4e was made to input and reverse a playback symbol clock, and was reversed is inputted into A-D converters 4c and 4d. Moreover, as shown in drawing 2 , it considers as the thing for data which sampled the coordinate transformation circuit 5 in the start of a playback symbol clock, and coordinate transformation circuit 5a for data newly sampled in the fall of a playback symbol clock is prepared. Furthermore, the fixed clock of the frequency of the symbol rate outputted from 8B is inputted into timing regenerative-circuit 7B.

[0064] Moreover, symbol frequency component generation section 71A which performs serial processing of a bit rate in timing regenerative-circuit 7B, and multiplication section 72A are changed into symbol frequency component generation section 71B which performs equivalent processing by the parallel processing of a symbol rate, and multiplication section 72B as each is shown in drawing 4 . Symbol frequency component generation section 71B samples the baseband phase data which sampled the baseband phase data sampled in the start of a playback symbol clock by 711d of D flip-flops in playback symbol clock falling, and were sampled in the fall of a playback symbol clock by D-flip-flop 711e in a playback symbol clock standup. 711f of subtractors subtracts the baseband phase data sampled in falling from 711d output, and 711g of subtractors subtracts the output of 711d from a 711e output. First data-conversion circuit 712A performs the same data conversion as the data-conversion circuit 712 of the gestalt 1 of operation to 711f output. Moreover, second data-conversion circuit 712B performs the same data conversion as the data-conversion circuit 712 of the gestalt 1 of operation to 711g output. Therefore, by the above-mentioned processing, the first data-conversion circuit 712A output deltathetaa (jT) is a formula (8a), and the second data-conversion circuit 712B output

deltathetab (jT) is a formula (8b), and it can express it.
deltathetaa(jT) =min {|theta(jT-T/2)-theta(jT) | and 2pi-|theta(jT-T/2)-theta(jT) |} (8a)
deltathetab(jT) =min {|theta(jT-T)-theta(jT-T/2) | and 2pi-|theta(jT-T)-theta(jT-T/2) |} (8a)
[0065] If multiplication section 72B subtracts deltathetab (jT) from this deltathetaa (jT) by subtractor 72c, value M (jT) which can be found from said formula (10) will be obtained. Moreover, it becomes unnecessary [the playback symbol clock generation section 75 of drawing 3] in drawing 4 , and the playback clock outputted from phase control section 7B turns into a playback symbol clock. Next, the changed part from phase phase control section 74A for realizing phase control section 74B is described. In control-section 74B, Hj which is the output of the amendment delay value calculation circuit 742 twice again about the numbers of bits m and n of the data bus in time delay setting signal calculation circuit 741,741A in phase phase control section 74A of the gestalt 1 of operation is doubled. Moreover, the fixed clock of a symbol rate is inputted into a clock phase-shifting circuit, and the number of clocks generated in the delay clock group generation circuit 7432 doubles a delay element by increasing twice. Moreover, the number of input clocks is doubled in the clock selection circuitry 7433.
[0066] Since the gestalt 2 of this operation can drop the frequency of an input clock on the frequency of a symbol rate from a rate twice the frequency of a symbol by the above modification, the clock frequency of the demodulator of the gestalt 2 of operation can serve as half [of the demodulator of the gestalt 1 of operation], can realize low-power-ization further, and can also make gate array-ization by CMOS of a demodulator easy.
[0067] Gestalt 3. drawing 13 of operation is drawing showing the configuration of the phase control section of a timing regenerative circuit which can perform phase control which could apply to the communication link which an always significant signal state follows continuously like an FDM communication link, and was stabilized. It is realizable by transposing the phase control section of the timing regenerative circuit in drawing 3 to the phase control section of the gestalt 3 of operation.
[0068] drawing 13 -- setting -- 743B -- the first clock phase-shifting circuit and 743C -- the second clock phase-shifting circuit and 744 -- a clock change judging circuit and 745 -- for an accumulation circuit and 746, as for a phase comparator circuit and 748, a clock selection circuitry and 747 are [a clock / an equalization circuit and 749] adders as for an error value accumulation circuit and 749a. Moreover, drawing 14 is drawing showing the example of a configuration of clock phase-shifting circuit 743B in drawing 13 , 743E is the first clock selection circuitry, and 743F are the second clock selection circuitry.
[0069] Although the rapid phase change of the playback clock to Kj-> (Kj**8) was given with the gestalt 1 of operation at the time of meaningless signal reception, since always significant data are received, the rapid phase change of the playback clock to Kj-> (Kj**8) cannot be given. Then, the phase control section in the gestalt 3 of this operation makes addition of the fixed value of "8 [**]" the adjustable value of "y [**]", asks for y which does not give the rapid phase change of a playback clock, and performs phase control to Kj-> (Kj**y). Actuation of a basis phase control section is explained referring to drawing 13 . Time delay setting signal calculation circuit 741A accumulates the timing phase error signal inputted, and adds an adder 749a output value from the accumulated value. If the circuit of time delay setting signal calculation circuit 741A is constituted and an adder 749a output value is set to y with a n-bit data bus, first time delay setting signal K1j which is a time delay setting signal calculation circuit 741A output can be found by the following formulas (23).
K1j= mod(K1j-1+Ej+y,2n) (23)
Moreover, the accumulation circuit 745 constitutes Ej from an accumulation circuit which consists of n-bit data buses considered as an input. The accumulation circuit 745 performs accumulation of the following formulas (24), and outputs the aggregate value as K2j.
K2j= mod(K2j-1+Ej,2n) (24)
[0070] It realizes by the same circuitry as clock phase-shifting circuit 743A of gestalt 1 publication of operation, and first clock phase-shifting circuit 743B and second clock phase-shifting circuit 743C consider a fixed clock twice the frequency of a symbol rate as an input. The first clock phase-shifting circuit and the second clock phase shift section circuit can also consist of circuits shown in drawing 14 . Like drawing 14 , since the delay clock group generation circuit 7432 is shared, a circuit scale is made small. Each of first clock selection-circuitry 743E and second clock selection-circuitry 743F is realizable by the same circuitry as clock selection-circuitry 743A. In first clock phase-shifting circuit 743B, if error time amount of the amount of delay of a delay element is set to alpha, the following formulas (25a) will be materialized from the input fixed clock of K1j and the playback 2 clock-doubling outputted from a clock selection circuitry to phase contrast deltap1 (radian).
deltap1=mod (pi / 2(n-1)+4alpha pi/T) (xK1j, 2pi)
(25a)
Similarly, if error time amount of the amount of delay of a delay element is set to alpha in second clock phase-shifting circuit 743C, the following formulas (26) will be materialized from the input fixed clock of K2j and the playback 2 clock-doubling outputted from a clock selection circuitry to phase contrast deltap2 (radian).
deltap2=mod (pi / 2(n-1)+4alpha pi/T) (xK2j, 2pi)
(26a)
Therefore, it will be set to deltap1=deltap2 if the relation of k1 j=K2j**8 is materialized in the case of alpha= 0 and n= 4.
[0071] Next, even when alpha is not "0", at least the clock in a basis phase control section makes relation between K1j and K2j K2 j=K1 j**y and adjustable, asks for y delta p1 and whose delta p2 correspond mostly, and gives the phase comparator circuit 747, the equalization circuit 748, the error value accumulation circuit 749, and adder 749a to time delay setting signal calculation circuit 741A. This the actuation of a series of is explained using the timing chart of drawing 15 . As shown in drawing 15 , the first delay clock presupposes that the phase is behind to the second delay clock. In this case, the value which sampled the second delay clock in the start of the first delay clock serves as logic "1." The value to which the first delay clock sampled the second

'delay clock in the start of the first delay clock when the phase was progressing to the second delay clock serves as logic "0." Therefore, the second delay clock is sampled in the start of the first delay clock, and as for the phase comparator circuit 747, at least a clock outputs PE=1, if a sampling value is logic "1" and a sampling value is logic "0" about PE=-1. The equalization circuit 148 equalizes PE, and if the average is forward and it is negative about logic "1", it outputs logic "-1." What is necessary is just to use for equalization a random walk filter, a moving-average filter, etc. which were mentioned above. Moreover, if the equalization circuit 148 has a sampling precision of the phase comparator circuit 747 as high as the clock of the preceding paragraph, it is unnecessary. Drawing 15 shows the case where the equalization circuit 748 is omitted. The error value accumulation circuit 749 carries out accumulation of the PE, and outputs an accumulation result. When it has the equalization circuit 148, the error value accumulation circuit 749 carries out accumulation of the output of the equalization circuit 148, "1", and "-1." In order that adder 749a may add this accumulation value and "8", y changes to "7" from "8" by time amount D. Therefore, since a time delay setting signal calculation circuit 741A output becomes the relation of "K1j+8" to "K1j+7, at the time of the time amount E of drawing 15 , the phase of the first delay clock progresses and phase contrast with the second delay clock is set to "0." In the example of drawing 15 , when K2j is "9", K1j changes to "0" from "1."

[0072] Moreover, when filling the following formulas (27) and the clock change judging circuit 744 in a basis phase control section does not fill the first delay clock, it gives the instruction which chooses the second delay clock as playback 2 clock-doubling, respectively.

$$\min\{K1j,15-K1j\} > \min\{K2j,15-K2j\} \quad (27)$$

In response to the instruction from the clock change judging section 744, the clock selection circuitry 746 chooses a clock and outputs it as playback 2 clock-doubling. In addition, the clock selection circuitry 746 considers as the same circuitry as the clock selection circuitry 7433 of the gestalt 1 of operation, it is asynchronous, and a clock phase shall not be confused even when a clock selection signal changes. By the above-mentioned processing, at the time of clock selection, the turbulence of the phase of playback 2 clock-doubling is not produced, even when alpha is not "0."

[0073] With the gestalt 3 of this operation, like the gestalt 1 of operation, a timing regenerative circuit inputs a twice as many fixed clock as a symbol rate, to a symbol period, is stabilized and realizes sufficiently small phase control step spacing (1/16 or less [of a symbol period]) from the above thing. Therefore, especially, when symbol rates, such as a high-speed radio-transmission system, are high, the timing regenerative circuit of the gestalt 3 of this operation can realize low-power-ization, and becomes easy [a circuit design]. Moreover, the timing regenerative circuit of the gestalt 3 of this operation can perform high-speed drawing in to a data pattern especially with large phase fluctuation by symbol frequency generation section 71A using the baseband phase data by which the exaggerated sample was carried out by the twice of a symbol rate. Furthermore, the timing regenerative circuit of the gestalt 3 of this operation can realize the phase control step which a phase change with a rapid playback clock phase did not arise, and was always stabilized, even when an always significant signal receive state continues continuously like an FDMA communication link by having the phase control section of the gestalt 3 of this operation.

[0074] The demodulator which has the phase control section of the gestalt 3 of operation which makes an input fixed clock the frequency of a symbol rate in time with gestalt 4. of operation is also realizable by easy circuit modification from the gestalt 3 of operation. Below, the changed part from the gestalt 3 of operation for operating the demodulator of the gestalt 3 of operation with the fixed clock of a symbol rate is described.

[0075] The configuration of the demodulator in the gestalt 4 of operation is the same as the configuration of the gestalt 2 of operation of drawing 2 . Moreover, the configuration of the timing regenerative circuit in the gestalt 4 of operation is the same as the configuration of the gestalt 2 of operation of drawing 4 . Only the configuration of the phase control section differs from the gestalt 2 of operation. First, modification parts other than the phase control section of the gestalt 3 of operation are performed like modification from the gestalt 1 of operation of the gestalt 2 of operation. next, the phase control section (drawing 13) of the gestalt 3 of operation -- setting -- time delay setting signal calculation circuit 741A and number-of-bits n of the data bus in the accumulation section 745 -- twice -- moreover, the fixed value "8" inputted into an adder is changed into "16." Furthermore, the fixed clock of a symbol rate is inputted into first clock phase-shifting circuit 743B and second clock phase-shifting circuit 743C, and the number of clocks generated in the delay clock group generation circuit 7432 doubles a delay element by increasing twice. Moreover, the number of input clocks is doubled in clock selection-circuitry 743E and clock selection-circuitry 743F.

[0076] By the above modification, since the gestalt 4 of this operation can drop the frequency of an input clock on the frequency of a symbol rate from a rate twice the frequency of a symbol, the clock frequency of the demodulator of the gestalt 4 of operation can serve as half [of the demodulator of the gestalt 3 of operation], and it can realize low-power-ization further, and can also make gate array-ization by CMOS of a demodulator easy.

[0077] Although the phase control section of the gestalt 3 of the gestalt 5. aforementioned implementation of operation realizes stable phase control like an FDMA communication link also when an always significant signal receive state continues continuously, it shows the phase control section which realizes phase control stabilized rather than the gestalt 3 of operation on a scale of a smaller circuit with the gestalt 5 of this operation.

[0078] The configuration of the demodulator in the gestalt 5 of operation is the same as the configuration of the gestalt 1 of operation of drawing 1 . Moreover, the configuration of the timing regenerative circuit in the gestalt 5 of operation is the same as the configuration of the gestalt 1 of operation of drawing 3 . Only the configuration of the phase control section differs from the gestalt 1 of operation. Drawing 16 shows the configuration of the phase control section by the gestalt 5 of operation. the inside of drawing, and 7400 -- for the second two frequency divider and 743A, a clock phase-shifting circuit and 7403 are [pi

phase-shifting circuit and 7401 / the first two frequency divider and 7402 / a clock change signal output circuit and 745A of a clock change circuit and 7404] accumulation circuits with a reset function.

[0079] Next, actuation of a basis phase control section is explained. The pi phase-shifting circuit 7400 carries out pi radian phase shift of the twice as many fixed clock as a symbol rate first. pi radian phase shift should just reverse a fixed clock with an inverter component etc. A fixed clock and the fixed clock by which pi radian phase shift was carried out are inputted into the clock change section 7403. The clock change circuit 7403 outputs the clock for a comparison, and one side for one of a fixed clock and the fixed clocks by which pi radian phase shift was carried out as a clock for phase shifts, respectively with the clock selection signal outputted from the latter clock change signal output circuit 7404. Accumulation circuit 745A consists of accumulation circuits of a n-bit data bus, carries out accumulation of the timing phase error signal by the formula (28a), and outputs the accumulation value Lj. Moreover, a register is reset to "0" like a formula (28b) by the reset signal Rj of the logic "0" outputted from the latter clock change signal output circuit 7404.

Lj= mod(Lj-1+Ej,2n) (Rj=1) (28a)

Lj= mod(Ej,2n) (Rj=0) (28b)

Clock phase-shifting circuit 743A carries out the clock for phase shifts deltap phase shift, as the clock for phase shifts is shown in a formula (29a) according to the accumulation value Lj, and it outputs it as playback 2 clock-doubling. It is referred to as n= 4 with the gestalt of this operation. Therefore, the relation between Lj and amount of phase shifts deltap serves as the following formulas (29b).

deltap=mod (2pi / 2(n-1)+4alpha pi/T) (xLj, 2pi)

(29a)

deltap=mod (pi / 4+4alpha pi/T) (xLj, 2pi) (29b)

The first two frequency divider 7401 carries out 2 dividing of the clock for a comparison, and outputs the clock after 2 dividing as a 2 dividing clock for a comparison. Moreover, the second two frequency divider 7402 carries out 2 dividing of the playback 2 clock-doubling, and outputs it as a playback 2 dividing clock.

[0080] The case of Lj=0 is considered here. In this case, as shown in drawing 17 (a), since the phase shift relation between the clock for a comparison and playback 2 clock-doubling is set to deltap=0, it is set to pi (radian). Therefore, the phase relation between 2 dividing clock for a comparison and a playback 2 dividing clock becomes pi/2 (radian). When retiming of the 2 dividing clock for a comparison is carried out with a playback 2 dividing clock at this time, the data Wj by which retiming was carried out show oar "1" and oar "0", as shown in drawing 17 (a). On the other hand, the case where Lj is changed is considered. In this case, the phase shift relation between the clock for a comparison and playback 2 clock-doubling is changed from pi (radian) by fluctuation of Lj. If Lj goes into the range of 12 >=Lj>=4, the data Wj which carried out retiming of the 2 dividing clock for a comparison with the playback 2 dividing clock will be changed from "1" to "0", or "0" to "1."

[0081] Lj increases drawing 17 (b), it is a timing chart when the phase of playback 2 clock-doubling is late gradually, and the phase contrast of playback 2 clock-doubling and the clock for a comparison decreases again through the jump of the phase of 0 ->2pi after decreasing to 0 in this case from pi. In this case, when it passes through the jump of the phase of 0 ->2pi, Data Wj are changed from "0" to "1." When changing this Wj, it notes that the phase contrast of the clock for a comparison and playback 2 clock-doubling has the relation which was mostly in agreement. The clock change signal output circuit 7404 will change the logic of the clock selection signal which is an output, if retiming of the 2 dividing clock for a comparison is carried out with a playback 2 dividing clock and the data Wj by which retiming was carried out are changed from "1" to "0", or "0" to "1." To coincidence, a reset signal Rj is made into logic "0" at the time of a change, and the register in accumulation circuit 745A is cleared.

[0082] For example, the clock change circuit 7403 presupposes at first that the fixed clock carried out pi phase shift considering the fixed clock as a clock for phase shifts was chosen, respectively as a clock for a comparison. If Wj is changed from "1" to "0", or "0" to "1" after that and the logic of a clock selection signal changes, the fixed clock used as the clock for a comparison pi phase shift will be changed so that a fixed clock may be chosen as the clock for phase shifts. The change of this clock is realized by the same circuitry as the clock selection circuitry 7433 of the gestalt 1 of operation (what is necessary is just to change the circuit which chooses one piece from eight clocks into the circuit which chooses one piece from two clocks). As mentioned above, since the phase contrast of the clock for a comparison and playback 2 clock-doubling at the time of a change has the relation which was mostly in agreement, the change of a phase with a rapid playback 2 clock-doubling phase is not produced at the time of a change.

[0083] When some conditions, for example, K1j, take the value before and behind "4" and K2j takes the value before and behind "12" like the gestalt 3 of operation, relational expression of a formula (27) is not materialized or Moreover, a sake, Although the change of a clock is frequently performed in the clock selection circuitry 746 and we are anxious about the increment in a clock jitter With the gestalt 5 of operation, since the timing after a clock change returns to the timing shown in drawing 17 (a), it shows the value in which Wj was again stabilized by oar "1" or oar "0." Therefore, also in case data are received continuously, operational stability can be expected from the phase control section of the gestalt 3 of operation. Furthermore, the phase control section of the gestalt 5 of operation can consist of the phase control sections of the gestalt 3 of operation in an easy circuit.

[0084] With the gestalt 5 of this operation, like the gestalt 1 of operation, a timing regenerative circuit inputs a twice as many fixed clock as a symbol rate, to a symbol period, is stabilized and realizes sufficiently small phase control step spacing (1/16 or less [of a symbol period]) from the above thing. Therefore, especially, when symbol rates, such as a high-speed radio-transmission system, are high, the timing regenerative circuit of the gestalt 5 of operation can realize low-power-ization, and becomes easy [a circuit design]. Moreover, the timing regenerative circuit of the gestalt 5 of operation can perform high-speed level luffing motion to a data pattern especially with large phase fluctuation by symbol frequency generation section

'71A using the baseband phase data by which the exaggerated sample was carried out by the twice of a symbol rate. Furthermore, the timing regenerative circuit of the gestalt 5 of operation can realize phase control which a phase change with a rapid playback clock phase did not arise, and was further stabilized from the timing regenerative circuit of the gestalt 3 of operation in a easier circuit, even when an always significant signal receive state continues continuously like an FDMA communication link by having the phase control section of the gestalt 5 of this operation.

[0085] The demodulator which has the phase control section of the gestalt 5 of operation which makes an input fixed clock the frequency of a symbol rate in time with gestalt 6. of operation is also realizable by easy circuit modification from the gestalt 5 of operation. Below, the changed part from the gestalt 5 of operation for operating the demodulator of the gestalt 5 of operation with the fixed clock of a symbol rate is described. The configuration of the demodulator in the gestalt 6 of operation is the same as the configuration of the gestalt 2 of operation of drawing 2 . Moreover, the configuration of the timing regenerative circuit in the gestalt 6 of operation is the same as the configuration of the gestalt 2 of operation of drawing 4 . Only the configuration of the phase control section differs from the gestalt 2 of operation.

[0086] First, modification parts other than the phase control section of the gestalt 5 of operation are performed like modification from the gestalt 1 of operation of the gestalt 2 of operation. Next, in the phase control section of the gestalt 5 of operation, number-of-bits n of the data bus in accumulation circuit 745A is doubled. Furthermore, the number of clocks which inputs the fixed clock of a symbol rate into the clock electronic switch circuit 7403 and the pi phase-shifting circuit 7400, and is generated to them in the delay clock group generation circuit 7432 in clock phase-shifting circuit 743A is doubled by increasing a delay element twice. Moreover, the number of input clocks is doubled in the clock selection circuitry 7433.

[0087] By the above modification, since the gestalt 6 of this operation can drop the frequency of an input clock on the frequency of a symbol rate from a rate twice the frequency of a symbol, the clock frequency of the demodulator of the gestalt 6 of operation can serve as half [of the demodulator of the gestalt 5 of operation], and it can realize low-power-ization further, and can also make gate array-ization by CMOS of a demodulator easy.

[0088] The phase control section of the gestalt 1 of the gestalt 7. aforementioned implementation of operation thru/or the gestalt 6 of operation was what generates two or more clocks and chooses one from the inside as playback 2 clock-doubling or a playback symbol clock using the delay element which carried out series connection each fundamentally. Therefore, by the control action prepared for every gestalt of each operation, if time delay error **alpha arises by a temperature change etc., although the abrupt change of the clock phase under significant signal reception is not produced, phase control step spacing will change. Therefore, the clock phase level-luffing-motion property and jitter property of each timing regenerative circuit which has the phase control section of the gestalt 1 of said operation thru/or the gestalt 6 of operation are somewhat influenced by the time delay error alpha. So, the gestalt 7 of operation shows the phase control section which does not use a delay element.

[0089] In the phase control section in the gestalt 7 of operation, phase control of playback 2 clock-doubling is performed using a quadrature modulation circuit. With the gestalt 1 of operation, the gestalt 3 of operation, and the gestalt 5 of operation, although the twice as many fixed clock as a symbol rate was considered as the input, the phase control section of the gestalt 7 of this operation considers a local sine wave signal twice the frequency of a symbol rate as an input instead of a twice as many fixed clock as a symbol rate. Therefore, the configuration of the demodulator in the gestalt 7 of operation turns into the configuration of having changed the fixed clock generator for timing playback which is twice the frequency of the symbol rate of 8A shown in drawing 1 into the fixed local sine wave oscillator for timing playback which is twice the frequency of a symbol rate. The configuration of the timing regenerative circuit in the gestalt 7 of operation is the same as the configuration of the gestalt 1 of operation of drawing 3 . Only the configuration of the phase control section differs from the gestalt 1 of operation.

[0090] the block diagram of the phase control section [in / in drawing 18 / the gestalt 7 of this operation] -- it is -- 745B -- an accumulation circuit and 7405 -- a cosine sign conversion circuit and 7406 -- for a DA converter and 7406c and 7406d, a low pass filter and 7406e and 7406f are [a quadrature modulation circuit and 7408 / a hard decision circuit, and 7406a and 7406b / an adder and 7406h of a multiplier and 7406g] pi/2 phase shifters.

[0091] Next, actuation of a basis phase control section is explained. If first the phase control number of steps is made into T/Z (T; a symbol period, Z= 2n), accumulation circuit 745B constitutes Ej from an accumulation circuit which consists of data buses of the bit considered as an input (n-1). Accumulation circuit 745B performs accumulation of the following formulas (30), and outputs the aggregate value as Pj.

Pj= mod(Pj-1+Ej,2n-1) (30)

The cosine sign conversion circuit 7405 outputs the following two digital data to Pj.

- Idj=cos (Pjxpi/4)
- Qdj=sin (Pjxpi/4) (31)

A quadrature modulation circuit carries out quadrature modulation of these data Idj and Qdj using a local sine wave signal twice the frequency of a symbol rate, and generates a modulating signal twice the frequency of a symbol rate. Although the quadrature modulation circuit was used for the means which carries out frequency conversion of the inphase component of the baseband signaling by which the PSK modulation was carried out conventionally, and the orthogonal component to the IF signal of a certain frequency, it uses this quadrature modulation circuit for the phase control section of playback 2 clock-doubling with the gestalt of this operation.

[0092] Detailed actuation of the quadrature modulation circuit 7406 is explained. First, as shown in drawing 18 , first, DA translation circuit 7406a carries out Idj, DA translation circuit 7406b carries out the DA translation of the Qdj, respectively, and low pass filters 7406c and 7406d remove the harmonic content of each analog signal by which the DA translation was carried out. If an I(t) low pass filter 7406d output is set to Q (t) for a low pass filter 7406c output, the signal SC (t) outputted from the

'quadrature modulation circuit 7406 will be searched for by the following formulas (32) from drawing 18 . (However, fs; symbol frequency)
SC(t) =I (t) xcos2pi(2fs) t +Q (t) xsin2pi(2fs) t (32)
Therefore, if SC (t) serves as a twice as many sine wave as a symbol frequency and it assumes that they are Idj** I (jT) and Qdj**Q (jT), as for phase contrast deltap from local signal cos2pi(2fs) t of Signal SC (t), and said Pj, the following formulas (33) will be materialized.
deltap=mod(Pj, 2n-1) xpi/4 (33)
The hard decision circuit 7408 outputs the signal of logic "0", when the amplitude of the above-mentioned SC (t) signal is forward and the amplitude of the above-mentioned SC (t) signal is negative about the signal of logic "1." Thus, if the hard decision of the above-mentioned SC (t) signal is carried out in the hard decision circuit 7408, playback 2 clock-doubling will be obtained. Therefore, the phase control section of the gestalt 7 of this operation always realizes clock phase control by the phase control step at equal intervals, in order not to use a delay element even when it is not influenced of the time delay error alpha but Pj increases with 6, 7, 0, 1, 2, and 3 --, and even when it decreases with 2, 1, 0, 7, 6, and 5 -- conversely.
[0093] From the above thing, in the gestalt 7 of this operation, a timing regenerative circuit inputs a twice as many local sine wave signal as a symbol rate, to a symbol period, is stabilized and realizes sufficiently small phase control step spacing (1/16 or less [of a symbol period]). Therefore, especially, when symbol rates, such as a high-speed radio-transmission system, are high, the timing regenerative circuit of the gestalt 7 of operation can realize low-power-ization, and becomes easy [a circuit design]. Moreover, the timing regenerative circuit of the gestalt 7 of operation can perform high-speed level luffing motion to a data pattern especially with large phase fluctuation by symbol frequency generation section 71A using the baseband phase data by which the exaggerated sample was carried out by the twice of a symbol rate. Furthermore, by the phase control section which has the quadrature modulation circuit of the gestalt 7 of this operation, a property does not make the timing regenerative circuit of the gestalt 7 of operation influence with temperature, but like an FDMA communication link, even when an always significant signal receive state continues continuously, it can realize stable phase control by the regular intervals playback symbol clock phase control step.
[0094] The demodulator which has the phase control section of the gestalt 7 of operation which makes an input local sine wave signal the frequency of a symbol rate in time with gestalt 8. of operation is also realizable by easy circuit modification from the gestalt 7 of operation. Below, the changed part from the gestalt 7 of operation for operating the demodulator of the gestalt 7 of operation by the local sine wave signal of a symbol rate is described. The configuration of the demodulator in the gestalt 8 of operation turns into the configuration of having changed the fixed clock generator for timing playback which is the frequency of the symbol rate of 8B shown in drawing 2 into the fixed local sine wave oscillator for timing playback which is the frequency of a symbol rate. The configuration of the timing regenerative circuit in the gestalt 8 of operation is the same as the configuration of the gestalt 2 of operation of drawing 4 . Only the configuration of the phase control section differs from the gestalt 2 of operation.
[0095] First, modification parts other than the phase control section of the gestalt 7 of operation are performed like modification from the gestalt 1 of operation of the gestalt 2 of operation. Next, accumulation circuit 745B is changed into the accumulation circuit which consists of data buses of the bit which considers Ej as an input (n-1), and consists of accumulation circuits with the n-bit data bus which considers Ej as an input. In this case, Pj can be found by the following formulas (34).
Pj= mod(Pj-1+Ej,2n) (34)
Moreover, processing of a formula (31) is changed into processing of the following formulas (35) in the cosine sign conversion circuit 7405.
- Idj=cos (Pjxpi/8)
- Qdj=sin (Pjxpi/8) (35)
Furthermore, a quadrature modulation circuit should just input the local sine wave signal of the frequency of a symbol rate instead of a local sine wave signal twice the frequency of a symbol rate. In this case, the signal SC (t) outputted from a quadrature modulation circuit is searched for by the following formulas (36) (however, fs; symbol frequency).
SC(t) =I(t) xcos2pi (fs) t +Q(t) xsin2pi (fs) t (36)
[0096] Therefore, with the gestalt 8 of operation, if SC (t) serves as a sine wave of a symbol frequency and it assumes that they are Idj** I (jT) and Qdj**Q (jT), as for phase contrast deltap from local signal cos2pi(fs) t of Signal SC (t), and said Pj, the following formulas (37) will be materialized.
deltap=mod(Pj, 2n) xpi/8 (37)
The hard decision circuit 7408 outputs the signal of logic "0", when the amplitude of the above-mentioned SC (t) signal is forward like the gestalt 7 of operation and the amplitude of the above-mentioned SC (t) signal is negative about the signal of logic "1." Thus, if the hard decision of the above-mentioned SC (t) signal is carried out in the hard decision circuit 7408, a playback symbol clock will be obtained.
[0097] By the above modification, since the gestalt 8 of this operation can drop the frequency of an input local sine wave signal on the frequency of a symbol rate from a rate twice the frequency of a symbol, the clock frequency of the demodulator of the gestalt 8 of operation can serve as half [of the demodulator of the gestalt 7 of operation], and it can realize low-power-ization further, and can also make gate array-ization by CMOS of a demodulator easy.
[0098] In order that a quadrature modulation circuit may take two DA converters to the phase control section of the gestalt 8 of the gestalt 9. aforementioned implementation of operation, its circuit scale is comparatively large. Furthermore, in order to use pi/2 phase-shifting circuit, degradation of a property is caused depending on the precision of pi/2 phase shift. So, with the gestalt 9 of operation, it is smaller than the gestalt 8 of operation, and the phase control section which was excellent in the property is

shown. The phase control section of the gestalt 9 of this operation considers a fixed clock twice the frequency of a symbol rate as an input like the gestalten 1, 3, and 5 of operation. However, the output of the phase control section of the gestalt 9 of operation is a point which is not playback 2 clock-doubling but a playback symbol clock as a different point from the old phase control section.

[0099] Therefore, the configuration of the demodulator in the gestalt 9 of operation turns into the configuration of having changed the fixed clock generator for timing playback which is the frequency of the symbol rate of 8B shown in drawing 2 into the fixed clock generator for timing playback which is twice the frequency of a symbol rate. Moreover, the configuration of the timing regenerative circuit in the gestalt 9 of operation is the same as the configuration of the gestalt 2 of operation of drawing 4 . Only the configuration of the phase control section differs from the gestalt 2 of operation. Drawing 19 which gave the same sign to the corresponding point with drawing 18 is the block diagram of the phase control section in the gestalt 9 of this operation, and, for the first sign inverter circuit and 7411, as for a clock amplitude value selection circuitry and 7413, the second sign inverter circuit and 7412 are [7409 / two frequency dividers and 7410 / a DA translation circuit and 7414] analog low-pass filtering circuits.

[0100] Next, actuation of a basis phase control section is explained. Like the gestalt 7 of operation, accumulation circuit 745B and the cosine sign conversion circuit 7405 perform accumulation according the timing phase error Ej to a formula (34), and ask for Data Idj and Qdj by conversion of a formula (35). Two frequency dividers 7409 carry out 2 dividing of the fixed clock twice the frequency of a symbol rate, and output the fixed clock by which 2 dividing was carried out. The first sign inverter circuit 7410 considers Idj as an input, and if the logic of the fixed clock by which outputted Idj as it was and 2 dividing was carried out if the logic of the fixed clock by which 2 dividing was carried out was "1" is "0", it reverses and outputs Idj. Similarly, the second sign inverter circuit 7411 considers Qdj as an input, and if the logic of the fixed clock by which outputted Qdj as it was and 2 dividing was carried out if the logic of the fixed clock by which 2 dividing was carried out was "1" is "0", it reverses and outputs Qdj. The clock amplitude value selection circuitry 7412 outputs the data of the first sign inverter circuit 7410, if a fixed clock twice the frequency of a symbol rate is logic "1", and if a fixed clock twice the frequency of a symbol rate is logic 0", it outputs the data of the second sign inverter circuit 7411.

[0101] If clock amplitude value selection-circuitry 7412 output value is set to Sd, a series of actuation so far will become like drawing 20 (the inside of drawing and T are symbol periods). When the timing of IdjQdj and the timing of the fixed clock to it twice the frequency of a symbol rate and the fixed clock by which 2 dividing was carried out are drawing 20 , the data sequence of Sd obtained by the above-mentioned processing serves as a wave which has a symbol frequency component like drawing 20 . The DA translation circuit 7413 carries out the DA translation of this Sd, and changes it into an analog signal. Furthermore, the analog low-pass filtering circuit 7414 removes the harmonic content of the signal after a DA translation, and outputs analog signal [after removal] s (t). The data sequence Sd is changed into curvilinear s (t) shown by the dotted line in the example of drawing 20 . Like the gestalt 7 of operation, the hard decision circuit 7408 carries out the hard decision of the s (t), and outputs the data after a hard decision as playback 2 clock-doubling. Like the example of drawing 20 , playback 2 clock-doubling falls at the forward -> negative changing point of signal s (t), and playback 2 clock-doubling starts at a negative -> forward changing point. Thus, like the gestalt 7 of operation, since a delay element is not used for the phase control section of the gestalt 9 of this operation, it is not influenced of the time delay error alpha, but always realizes clock phase control by the phase control step at equal intervals.

[0102] From the above thing, in the gestalt 9 of this operation, a timing regenerative circuit inputs a twice as many local sine wave signal as a symbol rate, to a symbol period, is stabilized and realizes sufficiently small phase control step spacing (1/16 or less [of a symbol period]). Therefore, especially, when symbol rates, such as a high-speed radio-transmission system, are high, the timing regenerative circuit of the gestalt 9 of operation can realize low-power-ization, and becomes easy [a circuit design]. Moreover, the timing regenerative circuit of the gestalt 9 of operation can perform high-speed level luffing motion to a data pattern especially with large phase fluctuation by symbol frequency generation section 71A using the baseband phase data by which the exaggerated sample was carried out by the twice of a symbol rate. Furthermore, by the phase control section which has the quadrature modulation circuit of the gestalt 9 of this operation, a property does not make the timing regenerative circuit of the gestalt 9 of operation influence with temperature, but like an FDMA communication link, even when an always significant signal receive state continues continuously, it can realize stable phase control by the regular intervals playback symbol clock phase control step. Moreover, the phase control section of the gestalt 9 of operation can constitute a DA converter and a low pass filter only from one piece, respectively, and in order to perform the remainder by digital signal processing, a circuit scale becomes small from the phase control section of the gestalt 7 of operation. Furthermore, a property is not influenced by the precision of analogue devices, such as pi/2 phase shifter, in order that the phase control section of the gestalt 9 of operation may perform processing equivalent to the quadrature modulation circuit 7406 of the gestalt 7 of operation by digital signal processing.

[0103] The timing regenerative circuit of the gestalt 1 of gestalt 10. implementation of operation realizes high-speed phase drawing in, when changing baseband phase data sharply for every symbol, but like pi / 4 shift QPSK modulation technique, when the amount of fluctuation of baseband phase data is comparatively small, it may require time amount for the level luffing motion of a timing phase. The gestalt 10 of operation shows the timing regenerative circuit which draws a timing phase in a high speed such even case.

[0104] The configuration of the demodulator in the gestalt 10 of operation is the same as the configuration of the gestalt 1 of operation of drawing 1 . The configuration of a timing regenerative circuit differs from the gestalt 1 of operation. Drawing 21 which attached the same sign as drawing 23 is the configuration of the timing regenerative circuit in the gestalt 10 of operation, and 78 is [the symbol frequency component generation section and 77A of a phase data interpolation circuit and 71C] the memory for filter information.

[0105] Next, actuation of the timing regenerative circuit in the gestalt 10 of operation is explained. This timing regenerative

circuit as well as the gestalt 1 of operation operates using the baseband phase data by which the exaggerated sample was carried out by the twice of a symbol rate, and a clock of operation is a fixed clock twice the frequency of a symbol rate. This timing regenerative circuit from baseband phase data theta i=theta (iT/2) (i= 1, 2, 3 and 4, --) by which over sampling technique was made twice the symbol rate By asking for the phase data theta between each sample phase data (2+T [iT/]/4) by interpolation processing of linear interpolation etc. The baseband phase data sequence by which over-sampling technique was carried out by 4 times of a symbol rate is generated, and a timing phase error is searched for like the conventional timing regenerative circuit using this data sequence. In addition, either of the gestalten 1, 3, 5, and 7 of operation should just be used for the phase control section of the gestalt 10 of this operation. Henceforth, detail actuation of the timing regenerative circuit of the gestalt 10 of this operation is explained.

[0106] Phase data assistant Mabe 78 of drawing 21 asks for the phase data theta between each sample phase data (2+T [iT/]/4) by the interpolation operation from the baseband phase data theta (iT/2) (i= 1, 2, 3 and 4, --). With the gestalt 10 of this operation, it asks for the phase data between each sample phase data by the linear interpolation of an easy phase. The processing in basis phase data assistant Mabe 78 is shown in a formula (38). However, deltaMi is the amount of fluctuation from theta (2+T [iT/]/2) to theta (iT/2), and can be found by the formula (39).

theta(2+T [iT/]/4) =mod (theta (iT/2))
+ deltaMi/2+2pi, 2pi (38)
delta Mi=theta (i+1) (T/2) - theta (iT/2)
[- pi<theta (i+1) (T/2)-theta(iT/2) <+pi]
delta Mi=theta (i+1) (T/2) - theta(iT/2) +2pi [- pi>=theta (i+1) (T/2)-theta (iT/2)]
delta Mi=theta (i+1) (T/2)-theta(iT/2)-2pi [+ pi<=theta (i+1) (T/2)-theta (iT/2)] (39)

With the gestalt of this operation, although linear interpolation was used for the interpolation operation, in addition as long as secondary interpolation etc. interpolates data, what kind of thing may be used.

[0107] Symbol frequency component generation section 71C calculates deltathetaR (iT/2) using the baseband phase data theta (iT/2) and the phase data theta in front of one (i-1) (T/2), as shown in the formula (40) shown below.

deltathetaR(iT/2) = min {|theta(iT/2)-theta(i-1) (T/2) | and 2pi-|theta(iT/2)-theta(i-1) (T/2) |} (40)

Moreover, as shown in the formula (41) shown below, deltathetaH (2+T [iT/]/4) is calculated using the phase data theta (2+T iT/]/4) which interpolated between each sample phase data, and the phase data theta (2-T [iT/]/4) which interpolated before one.

deltathetaH(2+T [iT/]/4) = min {|theta(2+T [iT/]/4)-theta(2-T [iT/]/4) | and 2pi-|theta(2+T [iT/]/4)-theta(2-T [iT/]/4) |} (41)

Therefore, data sequence deltatheta (kT/4) (k= 1, 2, 3 and 4, --) which has the symbol frequency component of a transmitting side can be found from the following formulas (42) to the timing of being 4 times much as a symbol rate.

deltatheta(kT/4) =deltathetaR (iT/2) [mod(k, 2) =0]
deltatheta(kT/4) =deltathetaH (2+T [iT/]/4)
[mod(k, 2) =1] (42)

[0108] In addition, the case where there are few amounts of symbol frequency components contained in deltathetaH (2+T [iT/]/4) than the amount of symbol frequency components contained in deltathetaR (iT/2) can be considered under the effect of a interpolation error. In that case, the weighting multiplier beta is applied to deltathetaH (2+T [iT/]/4). In this case, a formula (42) is changed into a formula (42a).

deltatheta(kT/4) =deltathetaR (iT/2) [mod(k, 2) =0]
deltatheta(kT/4) =betadeltathetaH (2+T [iT/]/4)
[mod(k, 2) =1] (42a)

[0109] Subsequent actuation is the same as the conventional example, and searches for correlation with deltatheta (kT/4) and the symbol frequency component of a receiving side in the complex multiplication section 72 and the low-pass filtering section 73. Moreover, if the timing phase contrast deltathetaj is computed, the value which negates deltathetaj will be inputted into the register of the accumulation circuits 745A and 745B of the time delay setting signal calculation circuits 741 and 741A of the gestalt 1 of operation thru/or the gestalt 4 of operation or the gestalt 5 of operation thru/or the gestalt 9 of operation, and phase simulation of the playback symbol clock will be carried out to transmit timing in an instant.

[0110] Thus, since it operates like [the demodulator shown in the gestalt 10 of this operation] the conventional example using the receiving PSK signal by which amplitude limiting was carried out, it can constitute from an easy circuit which has a limiter in the preceding paragraph, and the miniaturization of a circuit can be realized. Moreover, since the demodulator shown in the gestalt 10 of this operation is the configuration of the feedback mold which performs an AD translation to the timing of playback 2 clock-doubling, it can operate by the twice of the symbol rate which is the sampling rate of the one half of the conventional example, and can realize low-power-ization. Furthermore, the conventional timing regenerative circuit 7 inputs a x times as many fixed clock as a symbol rate, to having performed 1/x of a symbol period of phase control steps, the timing regenerative circuit shown in the gestalt 10 of this operation inputs a twice as many fixed clock as a symbol rate, to a symbol period, it is stabilized and sufficiently small phase control step spacing (1/16 or less [of a symbol period]) is realized. Therefore, especially, when symbol rates, such as a high-speed radio-transmission system, are high, a timing regenerative circuit can realize low-power-ization and becomes easy [a circuit design]. Moreover, the baseband phase data by which the exaggerated sample was made twice the symbol rate are used for a timing regenerative circuit by phase data assistant Mabe 78. In order to search for timing phase contrast like the conventional method using the baseband phase data which generated baseband phase data to the timing of being 4 times much as a symbol rate, and were generated to this timing of being 4 times many as this, Like the baseband

phase data by which pi / 4 shift QPSK modulation was carried out especially, phase fluctuation can perform high-speed drawing in to a comparatively small data pattern.
[0111]
[Effect of the Invention] As mentioned above, since the data sequence containing the symbol frequency component of a transmitting side can be acquired from the baseband phase data by which the exaggerated sample was made twice the symbol rate by 1 / easy signal processing which includes subtraction of difference 2 symbol according to this invention, digital-circuit-izing of this symbol frequency generation section and LSI-ization are easily realizable. Moreover, the timing regenerative circuit which shows a high-speed phase level-luffing-motion property is realizable by using this data sequence for timing playback. Furthermore, in order that this symbol frequency generation section may operate at a rate twice the frequency of a symbol, especially in a high-speed radio-transmission system, it can attain low-power-ization of a timing regenerative circuit, and it becomes easy to LSI-ize [of a timing regenerative circuit] it.
[0112] Furthermore, according to the next invention, since the playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side is generable, a timing regenerative circuit is realizable with the configuration of the feedback mold which considers the baseband phase data by which the exaggerated sample was made twice the symbol rate as an input in addition to ****, on a scale of a small circuit. Furthermore, the timing regenerative circuit which shows a high-speed phase level-luffing-motion property to the data pattern which repeats phase fluctuation of +pi and -pi for every symbol is realized.

[0113] Furthermore, since according to the next invention in addition to **** the random walk filtering section is used for the low-pass filtering section and multiplication data are equalized, the configuration of the low-pass filtering section becomes simple, and the timing regenerative circuit where a circuit scale is still smaller can be realized.
[0114] Furthermore, in order according to the next invention for the interpolation operation of a phase to generate a 4 times as many data sequence as the symbol rate which has a symbol frequency component in addition to ****, to perform a correlation operation with the symbol frequency component of a receiving side and to search for a timing phase error, the timing regenerative circuit which shows a high-speed phase level-luffing-motion property is realize to data with comparatively small phase fluctuation like baseband signaling by which pi / 4 shift QPSK modulation was carried out especially.
[0115] Moreover, according to the next invention, in order to operate with a fixed clock twice the frequency of a symbol rate, especially in a high-speed radio-transmission system, a timing regenerative circuit can attain low-power-ization of a timing regenerative circuit, and it becomes easy to LSI-ize [of a timing regenerative circuit] it.
[0116] Furthermore, according to the next invention, in order that a timing regenerative circuit may operate with the fixed clock of the same frequency as a symbol rate in addition to ****, low-power-ization of a timing regenerative circuit can be attained further and LSI-izing [of a timing regenerative circuit] becomes still easier.
[0117] Moreover, according to the next invention, a timing regenerative circuit operates with a fixed clock twice the frequency of a symbol rate, and realizes the timing regenerative circuit where a timing phase is not confused at the time of phase control and which realizes stable clock phase control during significant data reception by the amendment delay value calculation circuit.
[0118] Furthermore, according to the next invention, in order that a timing regenerative circuit may operate with the fixed clock of the same frequency as a symbol rate in addition to ****, low-power-ization of a timing regenerative circuit can be attained further and LSI-izing [of a timing regenerative circuit] becomes still easier.
[0119] Moreover, even when the error of the setting time delay by the temperature characteristic which generates the playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side continuously using two clock phase-shifting circuits, and is produced in a clock phase-shifting circuit arises according to the next invention, the timing regenerative circuit where a clock phase is not confused at the time of phase control is realized. Furthermore, with a fixed clock twice the frequency of a symbol rate, since a timing regenerative circuit operates, low-power-ization of a timing regenerative circuit can be attained especially in a high-speed radio-transmission system, and LSI-ization of a timing regenerative circuit becomes easy.
[0120] Furthermore, according to the next invention, in order that a timing regenerative circuit may operate with the fixed clock of the same frequency as a symbol rate in addition to ****, low-power-ization of a timing regenerative circuit can be attained further and LSI-izing [of a timing regenerative circuit] becomes still easier.
[0121] Moreover, even when the error of the setting time delay by the temperature characteristic which generates the playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side continuously by the easy circuitry using one clock phase-shifting circuit, and is produced in a clock phase-shifting circuit arises according to the next invention, the timing regenerative circuit where a clock phase is not confused at the time of phase control is realized. Furthermore, with a fixed clock twice the frequency of a symbol rate, since a timing regenerative circuit operates, low-power-ization of a timing regenerative circuit can be attained especially in a high-speed radio-transmission system, and LSI-ization of a timing regenerative circuit becomes easy.
[0122] Furthermore, according to the next invention, in order that a timing regenerative circuit may operate with the fixed clock of the same frequency as a symbol rate in addition to ****, low-power-ization of a timing regenerative circuit can be attained further and LSI-izing [of a timing regenerative circuit] becomes still easier.
[0123] Furthermore, according to the next invention, since the amount of delay in a fixed clock is given by choosing one from the clock of N individual which generates **** for individuals (N-1), and the delayed fixed clock of an individual (N-1) for a delay element in a clock phase-shifting circuit in addition to ****, and contains a fixed clock, a clock phase-shifting circuit is realizable in the simple circuit which does not need a high-speed clock.

[0124] Moreover, according to the next invention, the phase control sections are the quadrature modulation circuit which consists of two DA converters, two low pass filters, two multipliers, and one adder, and an easy circuit by the hard decision circuit, and can perform continuously playback clock phase control according to a time delay setting signal at intervals of a fixed phase control step. Furthermore, by the local sine wave twice the frequency of a symbol rate, in order that a timing regenerative circuit may operate, especially in a high-speed radio-transmission system, it can attain low-power-ization of a timing regenerative circuit, and it becomes easy to LSI-ize [of a timing regenerative circuit] it.
[0125] Furthermore, according to the next invention, in order that a timing regenerative circuit may operate by the local sine wave of the same frequency as a symbol rate in addition to ****, low-power-ization of a timing regenerative circuit can be attained further and LSI-izing [of a timing regenerative circuit] becomes still easier.
[0126] Moreover, according to the next invention, the phase control section is the easy circuit which consists of the digital circuit and the one DA translation section which perform processing equivalent to a quadrature modulation circuit, the one analog low-pass filtering section, and a hard decision circuit, and can perform continuously playback clock phase control according to a time delay setting signal at intervals of a fixed phase control step. Furthermore, by the local sine wave twice the frequency of a symbol rate, in order that a timing regenerative circuit may operate, especially in a high-speed radio-transmission system, it can attain low-power-ization of a timing regenerative circuit, and it becomes easy to LSI-ize [of a timing regenerative circuit] it.
[0127] Moreover, according to the next invention, the demodulator which outputs the recovery data which generated quickly the playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side, and synchronized with it is realized. Moreover, in order that this demodulator may operate using the baseband signaling by which amplitude limiting was carried out, it can have limiter amplifier in the preceding paragraph, and realizes the miniaturization of a demodulator. Furthermore, in order that this demodulator may make the exaggerated sample of the data twice a symbol rate, especially in a high-speed radio-transmission system, it can attain low-power-ization of a demodulator and it becomes easy to LSI-ize [of a demodulator] it.
[0128] Moreover, according to the next invention, the demodulator which outputs the recovery data which generated the playback symbol clock which made the exaggerated sample of the baseband signaling by which amplitude limiting was carried out twice the symbol rate, and carried out phase simulation to the transmission timing of a transmitting side, and synchronized with it is realized. Furthermore, in order that this demodulator may operate by the fixed clock twice the frequency of a symbol rate, or the local sine wave twice the frequency of a symbol rate, especially in a high-speed radio-transmission system, it can attain low-power-ization of a demodulator and it becomes easy to LSI-ize [of a demodulator] it.
[0129] Furthermore, according to the next invention, in addition to ****, a baseband inphase signal and a baseband rectangular cross signal are sampled in the standup and falling of a playback symbol clock., respectively Baseband inphase data, Although the number of the A-D converters used for a sampling increases from two conventional pieces to four pieces by the sampling circuit outputted as baseband rectangular cross data Since the frequency of a fixed clock or a local sine wave is reducible in the same frequency as a symbol rate from a rate twice the frequency of a symbol, low-power-ization of a demodulator can be attained further and also LSI-ization can realize an easy demodulator.

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] the baseband phase data by which the exaggerated sample was made twice the symbol rate -- 1/2 symbol -- difference -- carrying out -- difference -- with phase contrast Wakebe who outputs a result as phase contrast part data Which of the phase contrast part absolute value data which carried out absolute value conversion of said phase contrast part data, and the value which subtracted said phase contrast part absolute value data from 2pi by the radian display, or the smaller one as symbol frequency component data The timing regenerative circuit characterized by having the symbol frequency generation section which has the data-conversion section outputted to the timing of being twice many as a symbol rate.
[Claim 2] The multiplication section which carries out the multiplication of the symbol frequency component outputted from the after-mentioned phase control section to said symbol frequency component data, and is outputted to them as multiplication data, The low-pass filtering section which equalizes said multiplication data and outputs the equalized data as a timing phase error signal, Based on said timing phase error signal, the symbol frequency component which is an output The timing regenerative circuit according to claim 1 which carries out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and is characterized by having the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock.
[Claim 3] Said low-pass filtering section is a timing regenerative circuit according to claim 2 characterized by having the random walk filtering section which equalizes said multiplication data.
[Claim 4] Two or more baseband phase data by which the exaggerated sample was made said twice continuous symbol rate are used. The phase data at the time of a symbol period / 4 are computed using a interpolation operation from each sampling point. Use a calculation value as phase interpolation data, and 1 / 2 symbol difference of said phase interpolation data are carried out. difference -- a result -- interpolation phase contrast part data -- carrying out -- the interpolation phase contrast part absolute value data which carried out absolute value conversion of said interpolation phase contrast part data -- Which of the value which subtracted said interpolation phase contrast part absolute value data from 2pi by the radian display, or the smaller one and as symbol frequency component interpolation data The symbol frequency component interpolation data calculation section outputted to the timing of being twice many as a symbol rate, The multiplication of the inphase component of the symbol frequency outputted to said symbol frequency component interpolation data from the after-mentioned phase control section is carried out. The complex multiplication section which carries out the multiplication of the orthogonal component of the symbol frequency which outputs as inphase multiplication data and is outputted to said symbol frequency component data from the after-mentioned phase control section, and is outputted as rectangular multiplication data, The first integral filtering section which equalizes said inphase multiplication data with the first integral mold filter, and is outputted as timing inphase data, The second integral filtering section which equalizes said rectangular multiplication data with the second integral mold filter, and is outputted as timing rectangular cross data, r symbol period with said timing inphase data and the arc tangent section which calculates the arc tangent value of said timing rectangular cross data In quest of a timing phase error signal, it outputs from said arc tangent value. To coincidence in said first integral mold filter The integrating filter control section which outputs the integrating filter set signal which sets the vector length which said timing inphase data and said timing rectangular cross data show, and resets said second integral mold filter, Based on said timing phase error signal, the symbol frequency component which is an output The timing regenerative circuit according to claim 1 which carries out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and is characterized by having the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock.
[Claim 5] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. Said phase control section is a timing regenerative circuit where only the time amount which can be found based on a timing phase error signal is delayed in a fixed clock, and is characterized by having the clock phase shift section which outputs the signal which carried out 2 dividing of the delayed fixed clock as said playback symbol clock.
[Claim 6] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. Said phase control section is a timing regenerative circuit where only the time amount which can be found based on a timing phase error signal is delayed in a fixed clock, and is characterized by having the clock phase shift section which uses the delayed fixed clock as said

playback symbol clock.

[Claim 7] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The value which said phase control section subtracted the after-mentioned amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with said time delay setting signal with the time delay setting signal calculation section outputted as a time delay setting signal It is the clock phase shift section which outputs the signal with which only the time amount which set up the fixed clock was delayed, used the delayed fixed clock as the playback clock, and carried out 2 dividing of said playback clock as said playback symbol clock, and under [significant data receiving] setting. When the time amount to which 0 is outputted as an amendment delay value, and said time delay setting signal exceeds one period of a fixed clock during meaningless data reception is shown When the time amount to which the value equivalent to one period of a fixed clock is outputted as an amendment delay value, and said time delay setting signal exceeds -1 period of a fixed clock is shown It is the timing regenerative circuit characterized by having the amendment delay value calculation section which outputs zero as an amendment delay value while the value equivalent to -1 period of a fixed clock is outputted as an amendment delay value and said time delay setting signal shows the time amount of less than **one period of a fixed clock.

[Claim 8] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The value which said phase control section subtracted the after-mentioned amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with said time delay setting signal with the time delay setting signal calculation section outputted as a time delay setting signal It is the clock phase shift section to which only the time amount which set up the fixed clock is delayed and outputs the delayed fixed clock as said playback symbol clock, and under [significant data receiving] setting. When the time amount to which 0 is outputted as an amendment delay value, and said time delay setting signal exceeds one period of a fixed clock during meaningless data reception is shown When the time amount to which the value equivalent to one period of a fixed clock is outputted as an amendment delay value, and said time delay setting signal exceeds -1 period of a fixed clock is shown It is the timing regenerative circuit characterized by having the amendment delay value calculation section which outputs zero as an amendment delay value while the value equivalent to -1 period of a fixed clock is outputted as an amendment delay value and said time delay setting signal shows the time amount of less than **one period of a fixed clock.

[Claim 9] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The value which said phase control section subtracted the after-mentioned amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with said time delay setting signal with the time delay setting signal calculation section outputted as first time delay setting signal The first clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as first delay clock, The value which carried out accumulation of the timing phase error signal with the second time delay setting signal calculation section outputted as second time delay setting signal, and said second time delay setting signal The second clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as second delay clock, The absolute value of the time difference of the time delay which the value of said first time delay setting signal shows, and the period of said fixed clock When smaller than the absolute value of the time difference of the time delay which the value of said second time delay setting signal shows, and the period of said fixed clock The clock change judging section which outputs the clock selection signal which specifies said second delay clock for said first delay clock when large, The clock selection section which outputs what chose one of said first delay clock and the second delay clock, and carried out 2 dividing of the clock after selection based on said clock selection signal as said playback symbol clock, At least whether said first delay clock phase is progressing or it is behind to said second delay clock, and the clock that detects and outputs detection information as a phase detecting signal A phase comparator, The equalization section which equalizes said phase detecting signal and outputs the equalized phase detecting signal, The timing regenerative circuit characterized by having the error value accumulation section which accumulates said equalized phase detecting signal, adds the time amount equivalent to this accumulation value, and the period of a fixed clock, and is outputted as an amendment delay value.

[Claim 10] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The value which said phase control section subtracted the after-mentioned amendment delay value from the timing phase error signal, and carried out accumulation of the subtraction result with said time delay setting signal with the time delay setting signal calculation section outputted as first time delay setting signal The first clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as first delay clock, The value which carried out accumulation of the timing phase error signal with the second time delay setting signal calculation section outputted as second time delay setting signal, and said second time delay setting signal The second clock phase shift section which only the time amount which set up the fixed clock is delayed and is outputted as second delay clock, The absolute value of the time difference of the time delay which the value of said first time delay setting signal shows, and the period of said fixed clock When smaller than the absolute value of the time difference of the time delay which the value of said second time delay setting signal shows, and the period of said fixed clock The clock change judging section which outputs the clock selection signal which specifies said second delay clock for said first delay clock when large, The

'clock selection section which chooses one of said first delay clock and the second delay clock, and outputs a choosing clock as said playback symbol clock based on said clock selection signal, At least whether said first delay clock phase is progressing or it is behind to said second delay clock, and the clock that detects and outputs detection information as a phase detecting signal A phase comparator, The equalization section which equalizes said phase detecting signal and outputs the equalized phase detecting signal, The timing regenerative circuit characterized by having the error value accumulation section which accumulates said equalized phase detecting signal, adds the time amount equivalent to this accumulation value, and the period of a fixed clock, and is outputted as an amendment delay value.

[Claim 11] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. Said phase control section a fixed clock pi phase shift by radian display the signal carried out with the after-mentioned clock selection signal with pi phase shift section outputted as a pi phase shift clock One of a fixed clock and the aforementioned pi phase shift clocks is made into the clock for a comparison. The clock change section which uses another side as the clock for phase shifts, and outputs it, respectively, The surplus value at the time of carrying out accumulation of said timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a fixed clock with said time delay setting signal with the accumulation section outputted as a time delay setting signal The clock phase shift section which outputs the signal with which only the time amount which set up said clock for phase shifts was delayed, used the delayed signal as the playback clock, and carried out 2 dividing of the playback clock as said playback symbol clock, The first 2-minute periphery which carries out 2 dividing of said clock for a comparison, and outputs the clock which carried out 2 dividing as a 2 dividing clock for a comparison, The second 2-minute periphery which carries out 2 dividing of said playback clock, and outputs the clock which carried out 2 dividing as a playback 2 dividing clock, When said 2 dividing clock for a comparison is sampled with said playback 2 dividing clock and change produces it to the sampled data The timing regenerative circuit characterized by having the clock change signal output part which outputs the reset signal which it is at the change time and resets the accumulation value of said accumulation circles to 0, and the clock selection signal with which it is at the change time, and logic "1" and logic "0" change.

[Claim 12] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. Said phase control section a fixed clock pi phase shift by radian display the signal carried out with the after-mentioned clock selection signal with pi phase shift section outputted as a pi phase shift clock One of a fixed clock and the aforementioned pi phase shift clocks is made into the clock for a comparison. The clock change section which uses another side as the clock for phase shifts, and outputs it, respectively, The surplus value at the time of carrying out accumulation of said timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of a fixed clock with said time delay setting signal with the accumulation section outputted as a time delay setting signal The clock phase shift section to which only the time amount which set up said clock for phase shifts is delayed, uses the delayed signal as a playback clock, and outputs a playback clock as said playback symbol clock, The first 2-minute periphery which carries out 2 dividing of said clock for a comparison, and outputs the clock which carried out 2 dividing as a 2 dividing clock for a comparison, The second 2-minute periphery which carries out 2 dividing of said playback clock, and outputs the clock which carried out 2 dividing as a playback 2 dividing clock, When said 2 dividing clock for a comparison is sampled with said playback 2 dividing clock and change produces it to the sampled data The timing regenerative circuit characterized by having the clock change signal output part which outputs the reset signal which it is at the change time and resets the accumulation value of said accumulation circles to 0, and the clock selection signal with which it is at the change time, and logic "1" and logic "0" change.

[Claim 13] Said clock phase shift section said fixed clock from time amount y to time amount yx (N-1) It delays by y time step and the delay clock of an individual (N-1) is generated. Said fixed clock, The delay clock group generation section which outputs the clock of N individual containing the delay clock of the aforementioned (N-1) individual as a delay clock group, The clock selection-signal generation section which generates and outputs a clock selection signal based on said time delay setting signal, Based on said clock selection signal, one is chosen from said delay clock group, and it has the clock selection section outputted as a delay clock. Said delay clock group generation section Claim 5 characterized by having the N delay sections which give a time delay y by the delay element, inputting said fixed clock into said delay section of N individual by which series connection was carried out, and generating the delay clock of N individual thru/or a timing regenerative circuit according to claim 12.

[Claim 14] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The accumulation section which outputs the surplus value at the time of said phase control section carrying out accumulation of said timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of the after-mentioned local sine wave as a time delay setting signal, The cosine value at the time of writing the value which said time delay setting signal shows with the phase to the period of the after-mentioned local sine wave, The cosine sign transducer which calculates a sign value and is outputted as cosine data and sign data, respectively, Quadrature modulation of said cosine data and said sign data is carried out by the local sine wave. The quadrature modulation section which outputs the signal by which quadrature modulation was carried out as a timing regenerative signal and which consists of two DA converters, two low pass filters, two multipliers, one adder, and one pi/2 phase shifter, The timing regenerative circuit characterized by having the hard decision section which outputs the signal which carried out the hard decision of said timing regenerative signal, and carried out 2 dividing of the data after a hard

'decision as said playback symbol clock.

[Claim 15] Based on a timing phase error signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The accumulation section which outputs the surplus value at the time of said phase control section carrying out accumulation of said timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of the after-mentioned local sine wave as a time delay setting signal, The cosine value at the time of writing the value which said time delay setting signal shows with the phase to the period of the after-mentioned local sine wave, The cosine sign transducer which calculates a sign value and is outputted as cosine data and sign data, respectively, Quadrature modulation of said cosine data and said sign data is carried out by the local sine wave. The quadrature modulation section which outputs the signal by which quadrature modulation was carried out as a timing regenerative signal and which consists of two DA converters, two low pass filters, two multipliers, one adder, and one pi/2 phase shifter, The timing regenerative circuit which carries out the hard decision of said timing regenerative signal, and is characterized by having the hard decision section which outputs the data after a hard decision as said playback symbol clock.

[Claim 16] Based on a timing phase contrast signal, the symbol frequency component which is an output Carry out phase control so that phase simulation may be carried out to the transmission timing of a transmitting side, and it has the phase control section which outputs the most significant bit of said symbol frequency component as a playback symbol clock. The accumulation section which outputs the surplus value at the time of said phase control section carrying out accumulation of said timing phase error signal, and doing the division of the value after accumulation by the time amount equivalent to one period of the after-mentioned fixed clock as a time delay setting signal, The cosine value at the time of writing the value which said time delay setting signal shows with the phase to the period of the after-mentioned fixed clock, The cosine sign transducer which calculates a sign value and is outputted as cosine data and sign data, respectively, 2 dividing of the 2 double fixed clock which has a clock twice the frequency of the after-mentioned playback is carried out. When the 2-minute periphery which generates a fixed clock, and the logic of said fixed clock are "1", The first sign pars inflexa which outputs said cosine data as it is, carries out the multiplication of "-1" to said cosine data, and outputs it to them when the logic of said fixed clock is "0", The second sign pars inflexa which outputs said sign data as it is when the logic of said fixed clock is "1", carries out the multiplication of "-1" to said sign data, and outputs it to them when the logic of said fixed clock is "0", When said 2 double fixed clock is logic "1", the output value of said first sign pars inflexa is outputted as playback timing data 4 times. The clock amplitude value selection section which outputs the output value of said second sign pars inflexa as timing playback data 4 times when said 2 double fixed clock is logic "0", The DA translation section which carries out the DA translation of the timing playback data said 4 times, and is changed into an analog timing signal, The analog low-pass filtering section which outputs the signal which carried out low-pass filtering of said analog timing signal, and removed harmonic content as a timing regenerative signal, The timing regenerative circuit which carries out the hard decision of said timing regenerative signal, and is characterized by having the hard decision section which outputs the data after a hard decision as said playback symbol clock.

[Claim 17] One timing regenerative circuit of the 4 publications from claim 2 which outputs the playback symbol clock which considered the baseband phase data by which the exaggerated sample was made twice the symbol rate as the input, and carried out phase simulation to the transmission timing of a transmitting side, Complex multiplication of the local signal which has the same frequency as an IF signal is carried out to the receiving IF signal by which the PSK modulation was carried out. The rectangular detection section which carries out low-pass filtering of the inphase component after complex multiplication, and the orthogonal component after complex multiplication, and is outputted as a baseband inphase signal and a baseband rectangular cross signal, respectively, The exaggerated sample of said baseband inphase signal and said baseband rectangular cross signal is carried out to the timing of being twice many as the symbol rate which synchronized with said playback symbol clock., respectively Baseband inphase data, The sampling section outputted as baseband rectangular cross data, and said baseband inphase data, With said playback symbol clock with the polar-coordinate transducer which carries out polar-coordinate conversion of said baseband rectangular cross data, and outputs the data after polar-coordinate conversion as baseband phase data The demodulator which latches said baseband phase data, judges recovery data and is characterized by having the data judging section to output from the phase data after a latch.

[Claim 18] The playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side is outputted. From said fixed clock twice the frequency of a symbol rate, or said local sine wave twice the frequency of a symbol rate Claim 5 which generates said playback symbol clock, claim 7, claim 9, claim 11, claim 14, and one of timing regenerative circuits according to claim 16, The receiving IF signal by which the PSK modulation was carried out to the receiving IF signal by which amplitude limiting was carried out to the amplitude-limiting section which carries out amplitude limiting Carry out complex multiplication of the local signal which has the same frequency as an IF signal, and low-pass filtering of the inphase component after complex multiplication and the orthogonal component after complex multiplication is carried out. The rectangular detection section outputted as a baseband inphase signal and a baseband rectangular cross signal, respectively, Said baseband inphase signal and said baseband rectangular cross signal are sampled with said playback clock., respectively Baseband inphase data, The sampling section outputted as baseband rectangular cross data, and said baseband inphase data, With said playback symbol clock with the polar-coordinate transducer which carries out polar-coordinate conversion of said baseband rectangular cross data, and outputs the data after polar-coordinate conversion as baseband phase data The demodulator which latches said baseband phase data, judges recovery data and is characterized by having the data judging section to output from the phase data after a latch.

[Claim 19] The playback symbol clock which carried out phase simulation to the transmission timing of a transmitting side is

outputted. From said fixed clock of the same frequency as a symbol rate, or said local sine wave of the same frequency as a symbol rate Claim 6 which generates said playback symbol clock, claim 8, claim 10, claim 12, and one of timing regenerative circuits according to claim 15, The receiving IF signal by which the PSK modulation was carried out to the receiving IF signal by which amplitude limiting was carried out to the amplitude-limiting section which carries out amplitude limiting Carry out complex multiplication of the local signal which has the same frequency as an IF signal, and low-pass filtering of the inphase component after complex multiplication and the orthogonal component after complex multiplication is carried out. The rectangular detection section outputted as a baseband inphase signal and a baseband rectangular cross signal, respectively, Said baseband inphase signal and said baseband rectangular cross signal are sampled in the standup and falling of said playback symbol clock., respectively Baseband inphase data, The sampling section outputted as baseband rectangular cross data, and said baseband inphase data, With said playback symbol clock with the polar-coordinate transducer which carries out polar-coordinate conversion of said baseband rectangular cross data, and outputs the data after polar-coordinate conversion as baseband phase data The demodulator which latches said baseband phase data, judges recovery data and is characterized by having the data judging section to output from the phase data after a latch.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the whole gestalt 1 configuration of operation of the demodulator by this invention.
[Drawing 2] It is the block diagram showing the whole gestalt 2 configuration of operation of the demodulator by this invention.
[Drawing 3] It is the block diagram showing the configuration of the timing regenerative circuit in the demodulator of drawing 1 .
[Drawing 4] It is the block diagram showing the configuration of the timing regenerative circuit in the demodulator of drawing 2 .
[Drawing 5] It is the block diagram in the timing regenerative circuit by this invention showing the phase control section of the gestalt 1 of operation.
[Drawing 6] Even if the time error of the delay element of the gestalt 1 of operation in the timing regenerative circuit by this invention arises, it is the block diagram showing the phase control section which turbulence of a clock phase does not produce.
[Drawing 7] It is the block diagram in the phase control section by this invention showing a clock phase-shifting circuit.
[Drawing 8] It is the timing chart with which explanation of actuation of the timing regenerative circuit of drawing 3 is presented.
[Drawing 9] It is the flow chart with which explanation of actuation of the random walk filter of the gestalt 1 of operation is presented.
[Drawing 10] It is the timing chart with which explanation of actuation of the clock phase-shifting circuit of drawing 7 is presented.
[Drawing 11] It is the timing chart with which explanation of the conventional clock selection actuation is presented.
[Drawing 12] It is the graph of a time delay setting signal pair clock phase contrast property at the time of carrying out parameter ** of the time delay error of a delay element in the phase control section of drawing 5 .
[Drawing 13] It is the block diagram in the timing regenerative circuit by this invention showing the phase control section of the gestalt 3 of operation.
[Drawing 14] It is the block diagram showing the first clock phase-shifting circuit and the second clock phase-shifting circuit in the phase control section of drawing 13 .
[Drawing 15] It is the timing chart with which explanation of actuation of the phase control section of drawing 13 is presented.
[Drawing 16] It is the block diagram in the timing regenerative circuit by this invention showing the phase control section of the gestalt 5 of operation.
[Drawing 17] It is the timing chart with which explanation of actuation of the phase control section of drawing 16 is presented.
[Drawing 18] It is the block diagram in the timing regenerative circuit by this invention showing the phase control section of the gestalt 7 of operation.
[Drawing 19] It is the block diagram in the timing regenerative circuit by this invention showing the phase control section of the gestalt 9 of operation.
[Drawing 20] It is the timing chart with which explanation of actuation of the phase control section of drawing 19 is presented.
[Drawing 21] It is the block diagram showing the whole gestalt 10 configuration of operation of the timing regenerative circuit by this invention.
[Drawing 22] It is the block diagram showing the conventional demodulator whole configuration.
[Drawing 23] It is the block diagram showing the conventional timing regenerative-circuit whole configuration.
[Drawing 24] It is the wave form chart in the conventional timing regenerative circuit with which explanation of actuation of the symbol frequency component generation section is presented.
[Drawing 25] It is the timing chart in the conventional timing regenerative circuit with which explanation of actuation of the phase control section is presented.
[Description of Notations]
1 Limiter
2 Rectangular Detector Circuit
3 Local Oscillator for Rectangular Detection
4 Sampling Circuit
5 Polar-Coordinate Conversion Circuit
6 Data Judging Circuit
7 7A Timing regenerative circuit
71 Symbol Frequency Component Generation Section
72 Multiplication Section

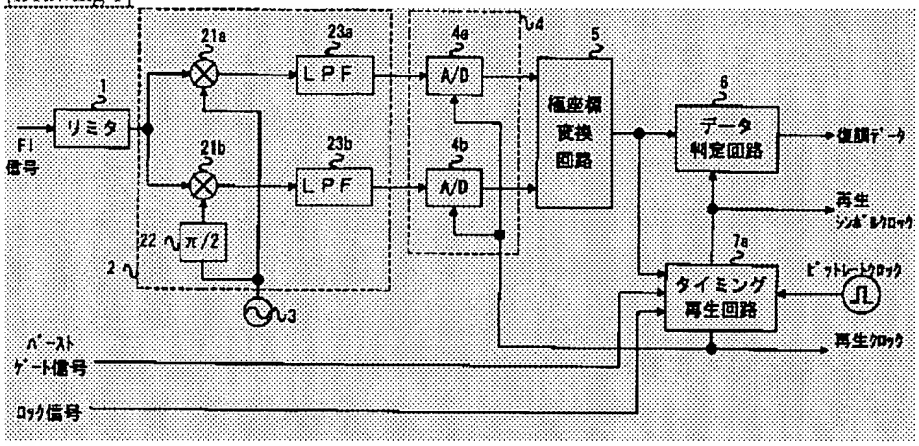
'73 Low-pass Filtering Section
74 Phase Control Section
75 Playback Symbol Clock Generation Section
76 Memory for Topology
77 Memory for Filter Information
78 Phase data assistant Mabe.

[Translation done.]

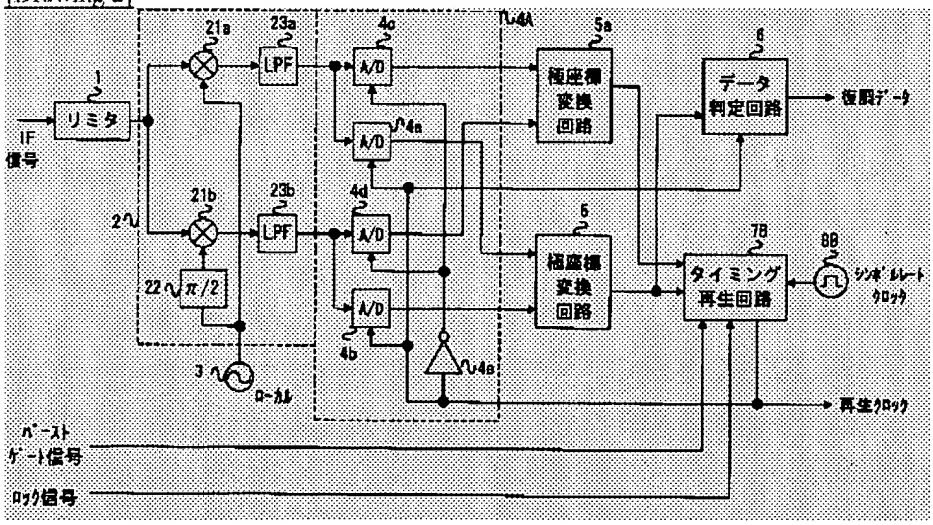
* NOTICES *

DRAWINGS

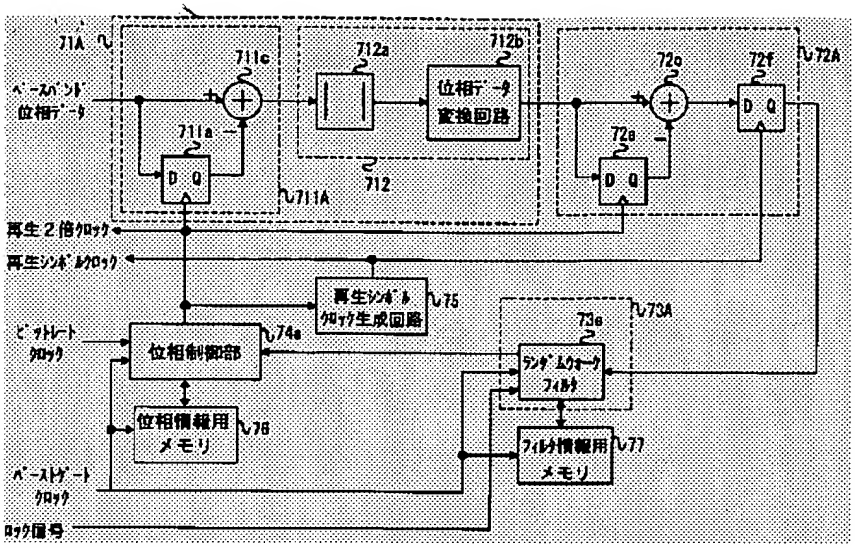
[Drawing 1]



[Drawing 2]



[Drawing 3]



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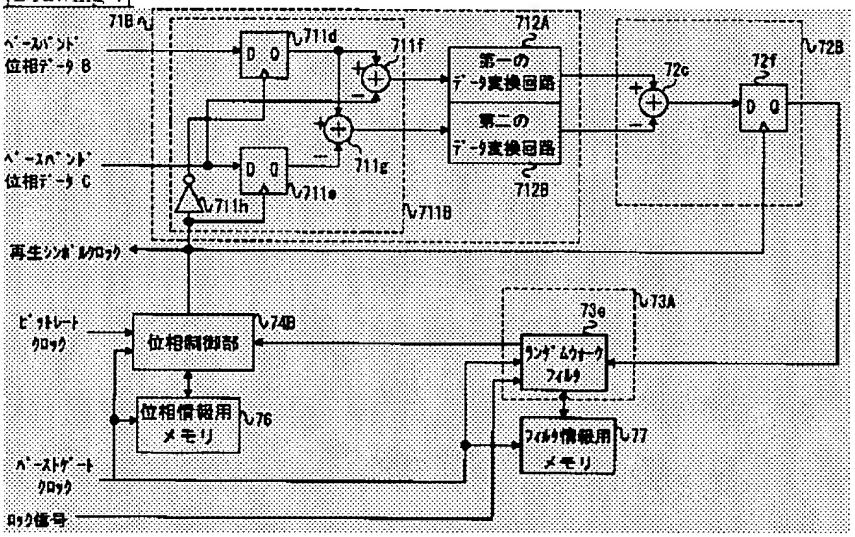

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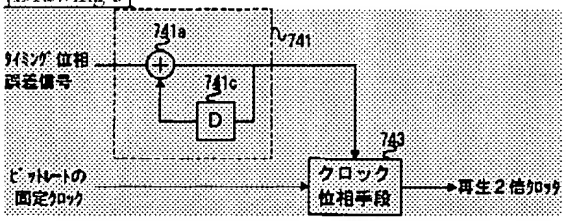

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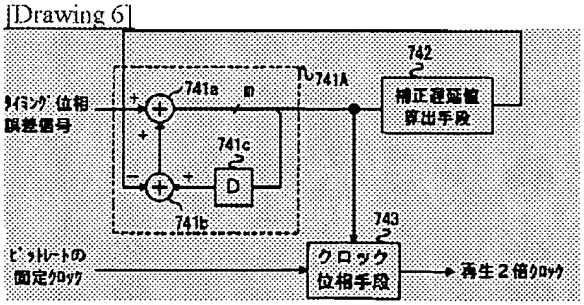

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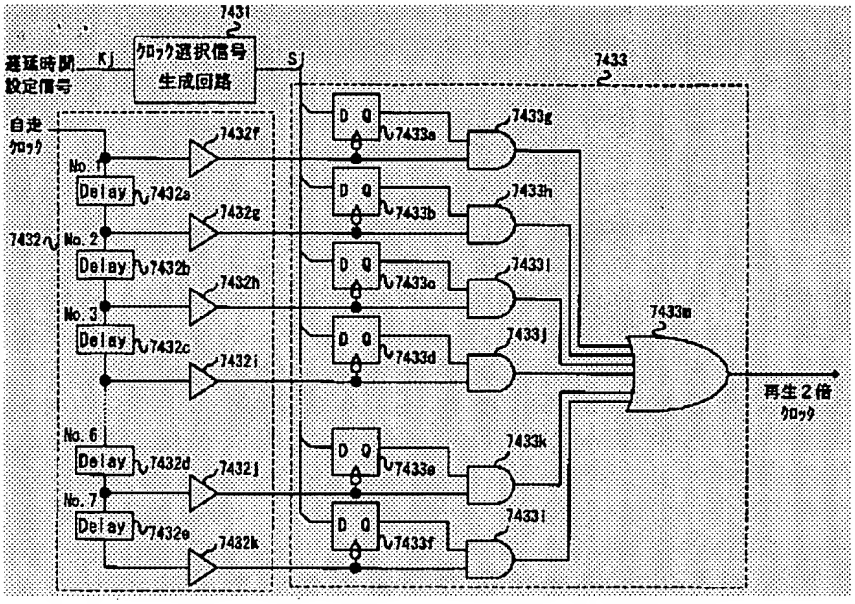

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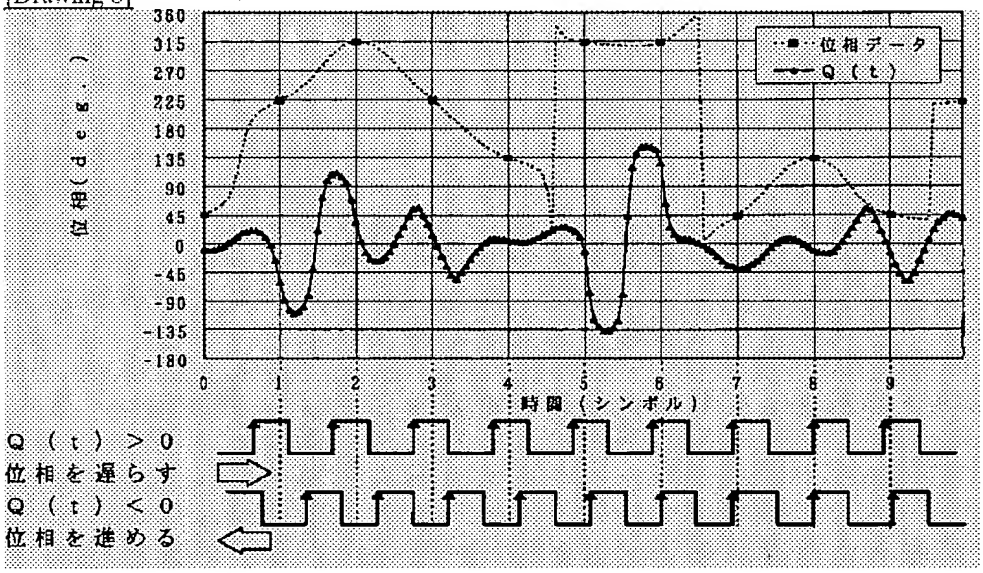
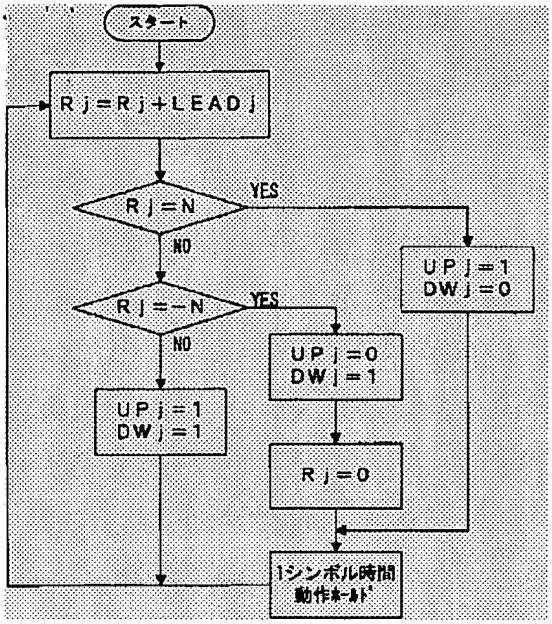


[Drawing 9]



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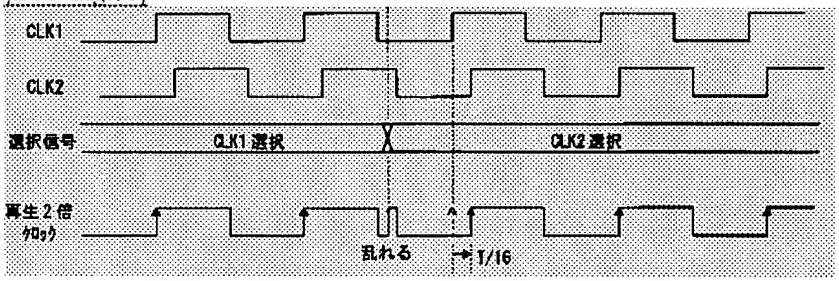

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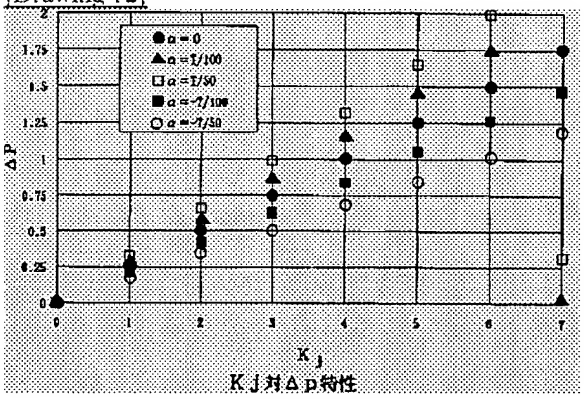
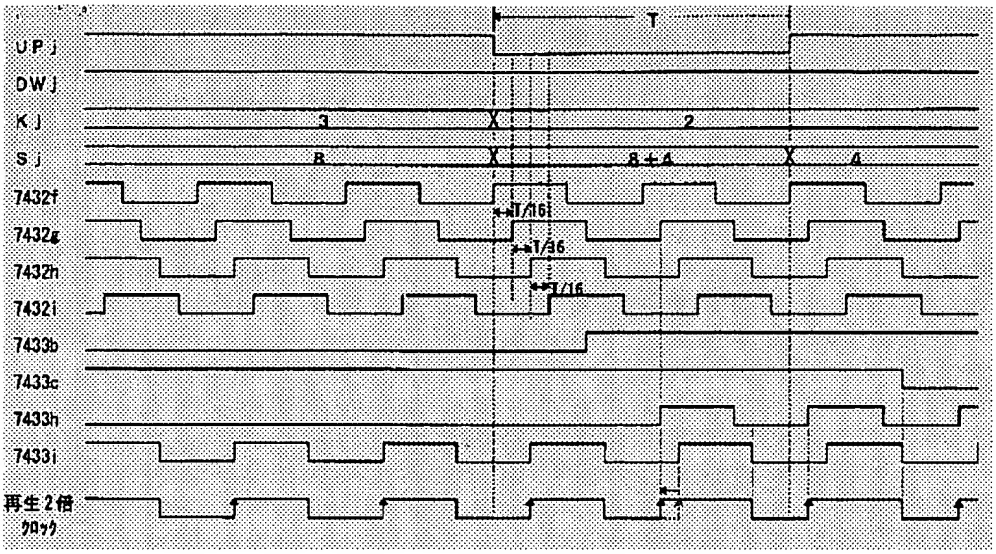
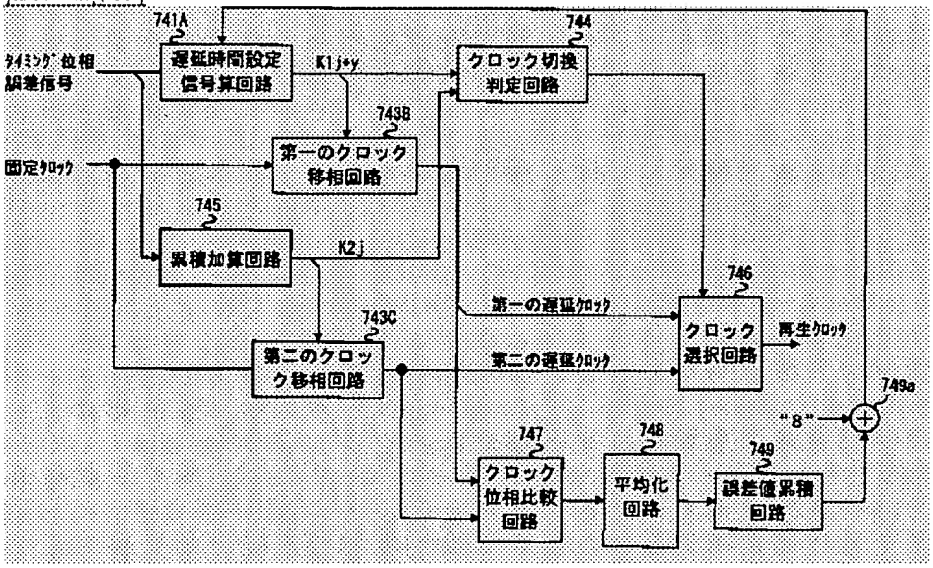


[Drawing 10]



[Drawing 13]



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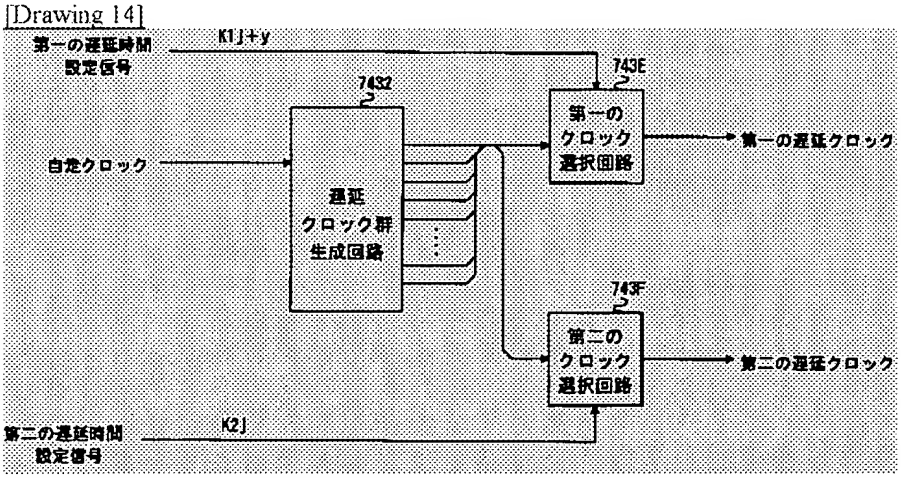

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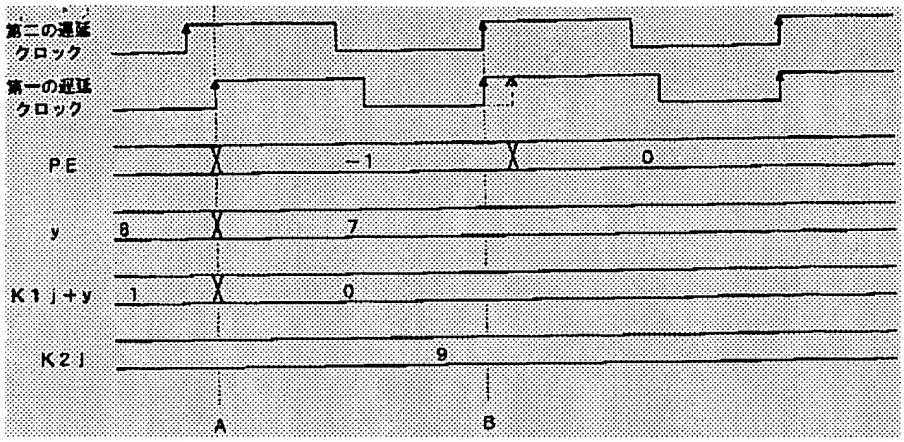

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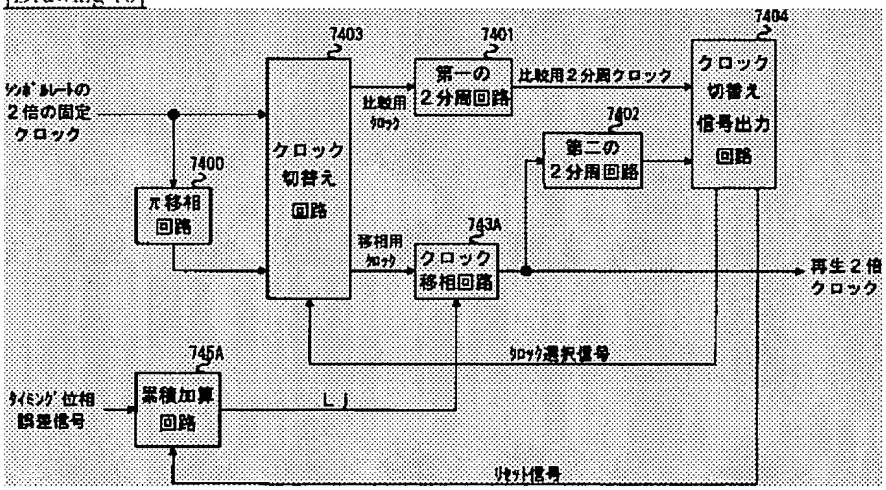

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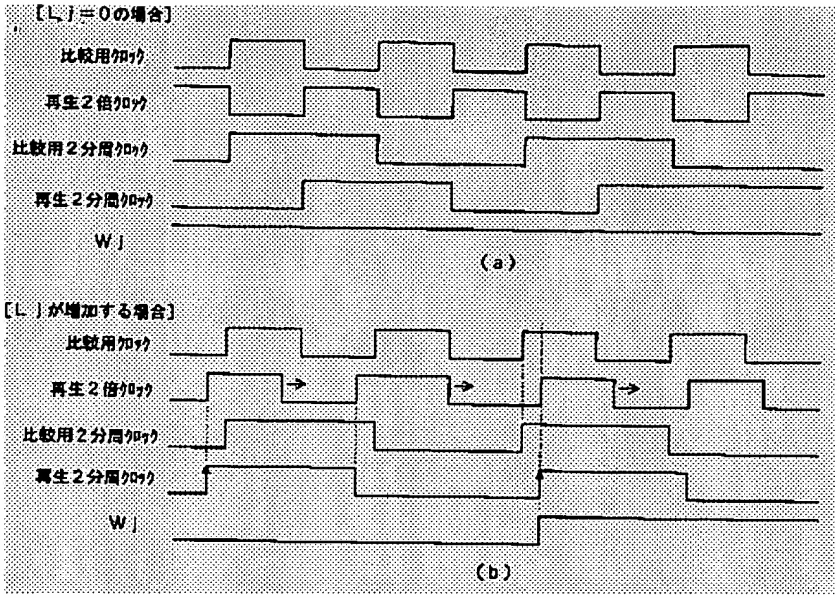

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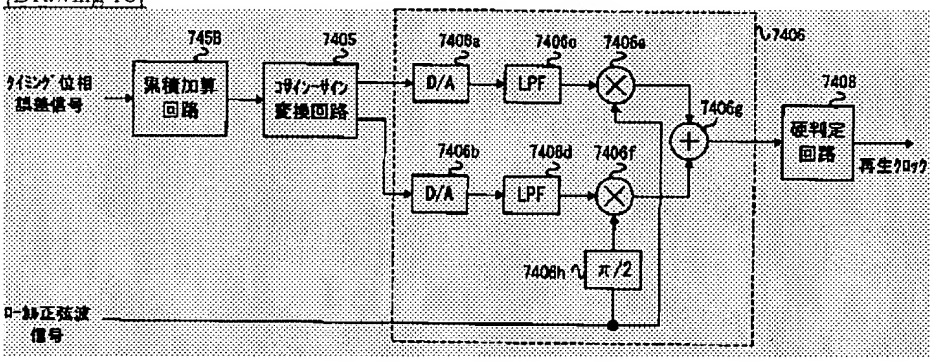
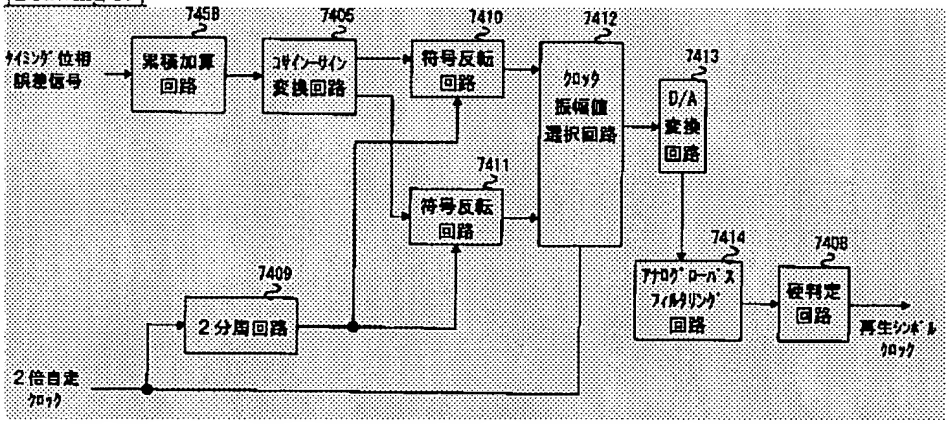


[Drawing 19]



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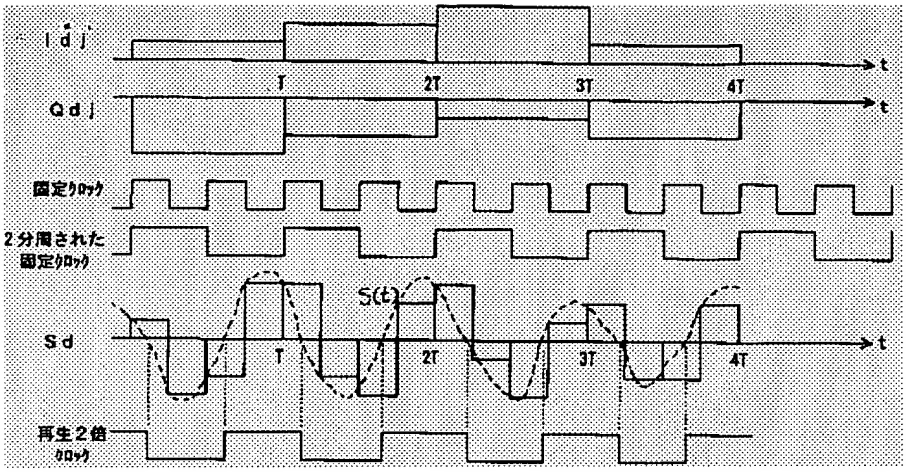

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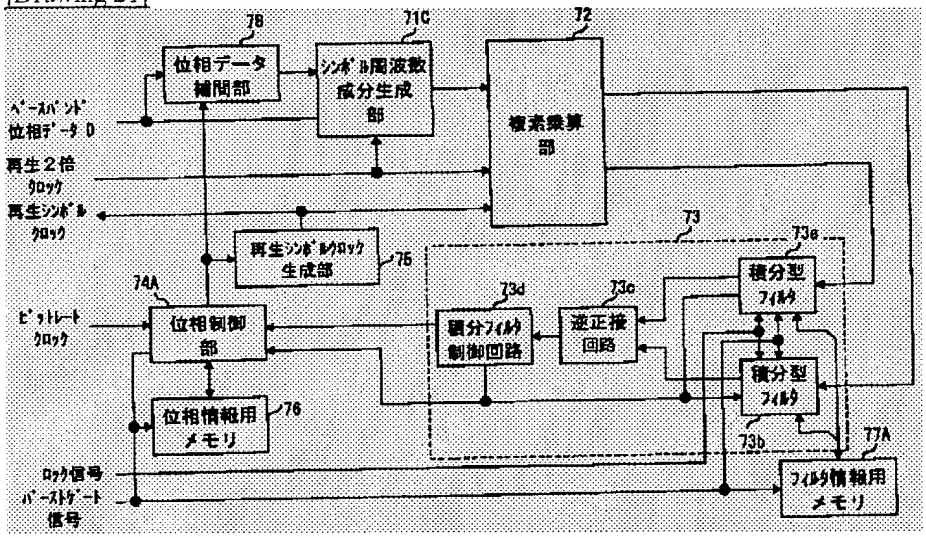

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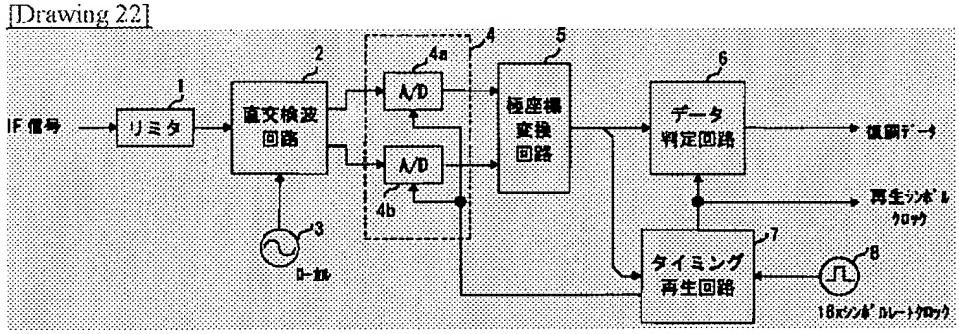

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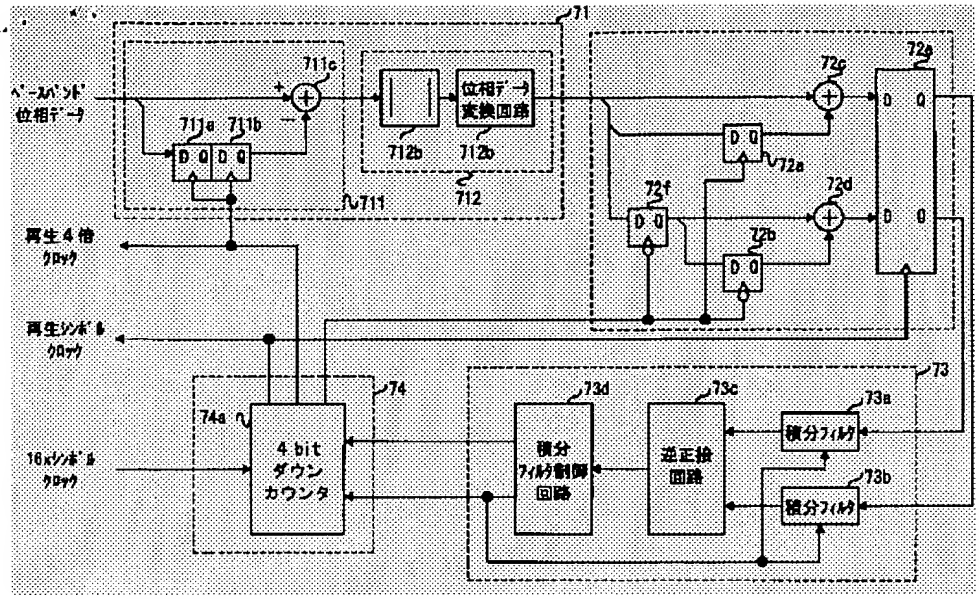

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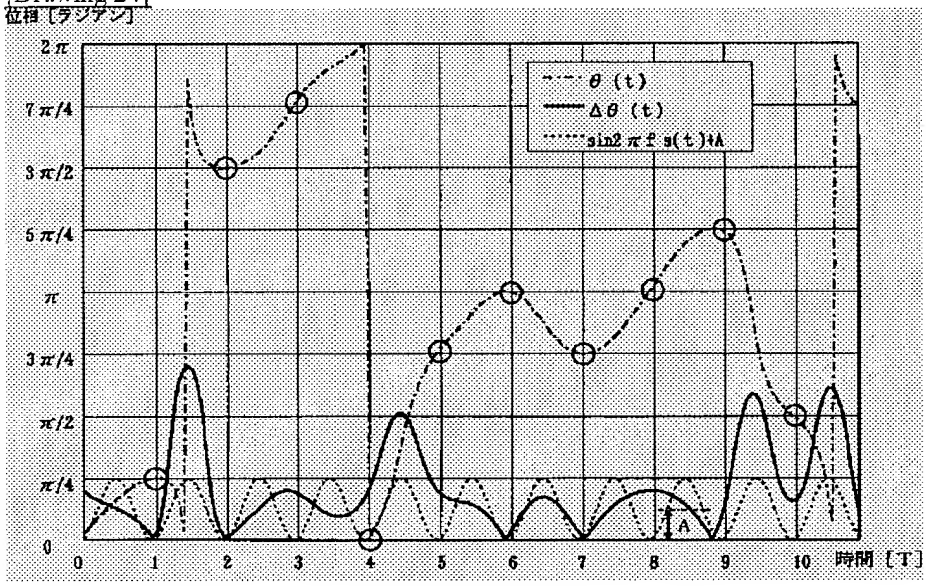

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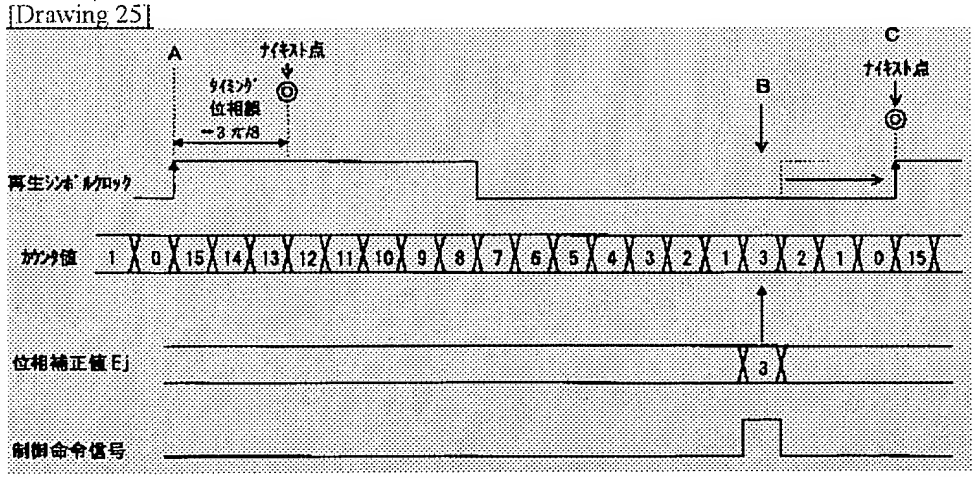

[Translation done.]